* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is applied to proof-pressure destructive prevention of the high proof-pressure IC which drives the bridge circuit of inverter equipment to an inverter equipment pan, and relates to an effective technique.
[0002]
[Description of the Prior Art] Conventionally, what was indicated by JP,4-54461,A as the current detection approach is known about the inverter circuit of a three phase circuit. The outline of the configuration of the three-phase-circuit inverter circuit indicated by the JP,4-54461,A is shown in drawing 15 . This three-phase-circuit inverter circuit has six switching elements T1 and T2 which consist of npn transistors, T3, T four, T5 and T6, each [these] switching elements T1 and T2 and T3, T four, and the electrical-potential-difference form inverter 1 that consists of six diodes D1, D2, D3, D4, D5, and D6 connected to juxtaposition T5 and T6, respectively.
[0003] Moreover, driving gears, such as a load of the motor 2 grade driven by this inverter circuit and six switching elements T1 and T2, T3, T four, and the high proof pressure IC (illustration abbreviation) that drives T5 and T6, are connected to this three-phase-circuit inverter circuit. Furthermore, the current detector 3 is formed in this three-phase-circuit inverter circuit. And the output voltage of the current detector 3 is changed into a digital signal by the A/D (analog/digital) transducer 4, and a processor (CPU) 5 is supplied. The interruption pulse generator 6 which generates the seizing signal of interrupt processing of this CPU5 is connected to CPU5. CPU5 is programmed to perform processing of predetermined interruption routine, if the current value detected by the current detector 3 turns into a predetermined value.
[0004] A switching element T1, T3, and T5 are the switching elements by the side of an upper arm (an upper arm switching element is called hereafter, respectively), respectively. A switching element T2, T four, and T6 are the switching elements by the side of a bottom arm (a bottom arm switching element is called hereafter, respectively), respectively. The upper arm switching element T1, the bottom arm switching element T2, upper arm switching element T3, bottom arm switching element T four and the upper arm switching element T5, and the bottom arm switching element T6 serve as a pair, respectively, and constitute the inverter of a three phase circuit.
[0005] Forward supply voltage is impressed to each up arm switching element T1, T3, and the collector of T5. Each up arm switching element T1, T3, and the emitter of T5 are connected to the bottom arm switching element T2, T four, and the collector of T6, respectively. Common connection of each Shimo arm switching element T2, T four, and the emitter of T6 is made, and they are connected to the negative supply voltage line through the current detector 3. Each up arm switching element T1, T3, T5 and each Shimo arm switching element T2, T four, and the gate of T6 are connected to the driving signal output terminal (illustration abbreviation) of driving gears, such as the high proof pressure IC, and each switching elements T1 and T2, T3, T four, and T5 and T6 are driven with the driving signal supplied from the driving gear (illustration abbreviation).

[0006] Moreover, the cathode of diodes D1, D3, and D5 is connected to each up arm switching element T1, T3, and the collector of T5, respectively, and the anode of diodes D1, D3, and D5 is connected to each up arm switching element T1, T3, and the emitter of T5, respectively. Moreover, the cathode of diodes D2, D4, and D6 is connected to each Shimo arm switching element T2, T four, and the collector of T6, respectively. The anode of diodes D2, D4, and D6 is connected to the direct negative supply voltage line, without minding the current detector 3. Namely, antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 is carried out to switching elements T1 and T2, T3, T four, and T5 and T6, respectively.

[0007] The three-phase-circuit inverter circuit shown in drawing 15 detects the current which comes to compound only each Shimo arm switching element T2, T four, and the current that flows T6 with the current detector 3 by being constituted as mentioned above. The inverter circuit of a configuration of being shown in this drawing 15 is often used conventionally.

[0008] The three-phase-circuit inverter circuit shown in drawing 16 forms the current detector 7 in the wiring path of a drive current of flowing for the load of motor 2 grade from this inverter circuit, instead of forming the current detector 3 between the bottom arm switching element T2, T four, and each emitter of T6 and a negative supply voltage line, as shown in drawing 15 . The configuration of the electrical-potential-difference form inverter 1 with which it comes to carry out antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 to six switching elements T1 and T2, T3, T four, and T5 and T6, respectively is the same as the configuration shown in drawing 15 . The inverter circuit of a configuration of being shown in this drawing 16 is also often used conventionally. In addition, although the illustration abbreviation was carried out, it cannot be overemphasized that A/D converter 4, CPU5, and the interruption pulse generator 6 are connected so that interrupt processing can be performed to the current detector 7 according to a detection current value.

[0009] The three-phase-circuit inverter circuit shown in drawing 17 forms the current detector 8 in the bus-bar which comes to make common connection of the bottom arm switching element T2, T four, and each emitter of T6, each anode of the diodes D2, D4, and D6 and each instead of forming the current detector 3 between the bottom arm switching element T2, T four, and each emitter of T6 and a negative supply voltage line, as shown in drawing 15 .

[0010] The configuration of the electrical-potential-difference form inverter 1 with which it comes to carry out antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 to six switching elements T1 and T2, T3, T four, and T5 and T6, respectively is the same as the configuration shown in drawing 15 . The inverter circuit of a configuration of being shown in this drawing 17 is also often used conventionally. In addition, although the illustration abbreviation was carried out, it cannot be overemphasized that A/D converter 4, CPU5, and the interruption pulse generator 6 are connected so that interrupt processing can be performed to the current detector 7 according to a detection current value.

[0011] The common single phase inverter equipment it was made to drive the arm switching element of the upper and lower sides of an inverter circuit with the high proof pressure IC is shown in drawing 18 . The single phase inverter circuit of this example is the thing of a configuration of being equivalent to the inverter part of the plane 1 of the three-phase-circuit inverter circuits shown in drawing 17 . That is, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.

[0012] And the current detector 106 is formed on the bus-bar with which common connection of the anode of the diode D2 by which antiparallel connection was carried out to the emitter of the bottom arm switching element T2 and it is made, and it results in the terminal by the side of negative (-) of DC power supply 108. Common connection of the cathode of the diode D1 by which antiparallel connection was carried out to the collector of the upper arm switching element T1 and it is made at the terminal by the side of forward (+) of DC power supply 108. A driving signal is inputted into each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2 from the high proof pressure IC 100, respectively.

[0013] Moreover, three external connection terminals P, U, and N are formed in the inverter circuit of the above-mentioned configuration. The external connection terminal P is the power supply terminal which impresses forward supply voltage to an inverter circuit, i.e., the terminal with which common connection of the collector of the upper arm switching element T1 and the cathode of diode D1 was made. The emitter of the power supply terminal T2 with which the external connection terminal N impresses negative supply voltage to an inverter circuit, i.e., a bottom arm switching element, and the anode of diode D2 are the terminals by which the other end of the current detector 106 by which common connection was made was connected to the end.
[0014] That is, the external connection terminal P is connected as a forward side in DC power supply 108 between the external connection terminal P and the external connection terminal U. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1. And between the external connection terminal U and the external connection terminal N, the reactor (inductance value: LL) 107 is connected as a load.
[0015] The parasitism reactor of L1 exists [an inductance value] in the wiring section between the connection node E1 and the collector of the bottom arm switching element T2. The parasitism reactor of L2 exists [an inductance value] in the cathode side wiring section of diode D2. The parasitism reactor of L3 and L4 exists [an inductance value] in a serial at the anode side wiring section of diode D2. The parasitism reactor of L5 exists [an inductance value] in wiring between the connection node E0 and the connection node N1 prepared in the opposite side (namely, between the current detector 106 and the external connection terminals N) of E0 on both sides of the current detector 106.
[0016] In addition, power-source body 108a and capacitor 108b which generate electromotive force are connected to juxtaposition, and DC power supply 108 are constituted.
[0017] The high proof pressure IC 100 The driving signal input terminals UPi and UNi of this IC100 are minded. The signal inputted from the outside The output signal of the input buffer a1 held temporarily, the level shifter a2 which generates the signal of the floating potential which received the output signal of the input buffer a1, and floated from the potential of the signal, and a level shifter a2 is received. The upper arm switching element T1 The detecting signal outputted from the bottom arm side driver circuit a4 which receives the output signal of the upper arm side driver circuit a3 to drive and an input buffer a1, and drives the bottom arm switching element T2, the overcurrent detector a5 which performs detection of an overcurrent, and the overcurrent detector a5 It has the error signal generator a6 which receives and generates an error signal.
[0018] The upper arm side driver circuit a3 outputs a driving signal to the upper arm switching element T1 through the upper arm switching element driving signal output terminal UPo prepared in the high proof pressure IC 100. Moreover, a forward and negative floating electrical potential difference is impressed to the high proof pressure IC 100 from the outside in the upper arm side driver circuit a3 through the floating power-source forward side input terminal VB 1 prepared, respectively and the floating power-source negative side input terminal VS 1. The floating power-source negative side input terminal VS 1 serves as the upper arm switching element driving signal criteria output terminal.
[0019] The bottom arm side driver circuit a4 outputs a driving signal to the bottom arm switching element T2 through the bottom arm switching element driving signal output terminal UNo prepared in the high proof pressure IC 100. Moreover, forward supply voltage is impressed to the bottom arm side driver circuit a4 from the outside through the forward side power supply terminal VCC prepared in the high proof pressure IC 100. The bottom arm side driver circuit a4 is connected to the bottom arm switching element driving signal criteria output terminal VS 0 prepared in the high proof pressure IC 100.
[0020] The overcurrent detector a5 is connected to the current detection terminal OC prepared in the high proof pressure IC 100.
[0021] The error signal generator a6 outputs an error signal to a control unit, an alarm information means, etc. which the exterior does not illustrate through the error output terminal Fo prepared in the high proof pressure IC 100.
[0022] The forward side power supply terminal VCC and the negative side power supply terminal VSS

which were prepared in the high proof pressure IC 100, respectively are connected to the positive electrode and negative electrode of an external power 101, respectively. And the negative side power supply terminal VSS is grounded.

[0023] External [of the diode 102, the capacitor 103, and reference diode 109 other than the above-mentioned external power 101] is carried out to the high proof pressure IC 100. Namely, the anode is connected to the forward side power supply terminal VCC, and, as for diode 102, the cathode is connected to the floating power-source forward side input terminal VB 1. The capacitor 103 is connected between the floating power-source forward side input terminal VB 1 and the floating power-source negative side input terminal VS 1. Reference diode 109 is formed in the overvoltage protections of the bottom arm switching element driving signal criteria output terminal VS 0, and is connected between the bottom arm switching element driving signal criteria output terminal VS 0 and the negative side power supply terminal VSS.

[0024] The high proof pressure IC 100 is connected to the inverter circuit which consists of the arm switching elements T1 and T2 and DC power supply 108 of a vertical pair as follows. That is, the floating power-source negative side input terminal (upper arm switching element driving signal criteria output terminal) VS 1 of the high proof pressure IC 100 is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1. The upper arm switching element driving signal output terminal UPo is connected to the gate G1 of the upper arm switching element T1 through gate resistance 104.

[0025] Moreover, the bottom arm switching element driving signal criteria output terminal VS 0 is connected to the connection node E0 by the side of the emitter of the bottom arm switching element T2. The bottom arm switching element driving signal output terminal UNo is connected to the gate G2 of the bottom arm switching element T2 through gate resistance 105. The current detection terminal OC is connected to said connection node E0. Moreover, the negative side power supply terminal VSS is connected to said connection node N1 of an inverter circuit. Since the current detector 106 is between these connection node E0 and the connection node N1 as mentioned above, the detection electrical potential difference of the current detector 106 will be impressed to the current detection terminal OC.

[0026] L6 and the parasitism reactor of L7 exist [the inductance value] in wiring between the bottom arm switching element driving signal criteria output terminal VS 0 and the connection node E0, and wiring between the negative side power supply terminal VSS and the connection node N1, respectively.

[0027] The maximum of pressure-proofing here of the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) +600] bolt extent, although there are some differences by the application, and the thing of the minimum value of any applications is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent. That is, between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, it means that the electrical potential difference not more than -5V cannot be applied.

[0028] Since this is guaranteed only about -0.5V to the potential below the supply voltage of the IC also by IC which generally consists of an IC which consists of CMOSFET(s) (insulated gate field effect transistor of a complementary type), or TTL (transistor transistor logic) of BAIPORA, it is considered to be because it to become weak theoretically to the potential below supply voltage.

[0029] The timing of the inverter equipment shown in drawing 18 of operation is shown in drawing 19 . In drawing 19 , S (UPo) and S (UNo) are the signals outputted from the upper arm switching element driving signal output terminal UPo of the high proof pressure IC 100, and the bottom arm switching element driving signal output terminal UNo, respectively, and are the driving signal of the upper arm switching element T1 and the bottom arm switching element T2, respectively. Moreover, the current on which I1 flows the upper arm switching element T1, the current to which I2 flows to diode D2, and I3 are currents which flow a reactor 107.

[0030] Each driving signal S (UPo) and S (UNo) of the up-and-down arm switching elements T1 and T2 of the up-and-down arm switching elements T1 and T2 is all an OFF state relatively in the condition of

low voltage (low) level (it considers as L level hereafter). Therefore, the driving signals S (UPo) and S (UNo) of L level are switching element off signals.

[0031] When driving signals S (UPo) and S (UNo) are all switching element off signals (namely, L level) If a driving signal S (UPo) starts and it changes to the signal (namely, switching element ON signal) of high potential (yes) level (it considers as H level hereafter) relatively While a driving signal S (UPo) is H level (period of A in drawing 19), a current flows through the external connection terminal P, the upper arm switching element T1, a reactor 107, and the external connection terminal N in the path of negative-electrode HE **** of DC power supply 108 from the positive electrode of DC power supply 108.

[0032] Here, in the inverter equipment shown in drawing 18 , if time amount width of face (period of A) Ton in case 3mH(s) and a driving signal S (UPo) are H level about the inductance value LL of 300V and a reactor 107 in the output voltage VDC of DC power supply 108 is set to 1ms, the peak current Ip of a reactor 107 will be set to 100A (ampere) from the following formula.

Ip=VDC-Ton/LL= {300and1- (E-3)} /{3- (E-3)}
=100[A]

In addition, that it is with "(E-n)" means - (minus) n-th power of 10 among this specification. However, n is the natural number.

[0033] Then, if a driving signal S (UPo) falls and it is set to L level, the upper arm switching element T1 will change to an OFF state. By it, the current I1 which flows the upper arm switching element T1 begins to decrease, and only predetermined time amount (period of B in drawing 19) is in it, and it becomes zero. On the other hand, the current I2 which flows diode D2 begins to increase synchronizing with the fall edge of a driving signal S (UPo), and reaches said peak current Ip after period progress of B. By the period of this B, since the variation (di/dt) per unit time amount of a current is large, several V induced voltage occurs also in few wiring inductances. Moreover, diode D2 will generate the ON state voltage of about 2v, if a current flows.

[0034] In the inverter equipment shown in drawing 18 here the synthetic inductance value of the wiring inductances L1, L2, L3, and L4 20nH(s), If switching speed Toff of 2V and the upper arm switching element T1 is set to 400ns for ON state voltage VF of diode D2 and value 100A of the above-mentioned peak current Ip is used The electrical potential difference V (E1-E0) built between the connection node E1 by the side of the emitter of the upper arm switching element T1 and the connection node E0 by the side of the emitter of the bottom arm switching element T2 is set to -7V from the following formula.

400and [V(E1-E0) =- (L1+L2+L3+L4) and Ip/Toff-VF=-{20-(E-9) -100}// {and / and (E-9) /}] -2=-7 [V]

[0035] Thus, even if a wiring inductance is small, if a high current flows like the period of B of drawing 19 , the electrical potential difference exceeding the pressure-proofing by the side of minus of the high proof pressure IC 100, i.e., [(potential of VS0) -5] bolt, (it is less than the minimum value) will occur.

[0036] Moreover, if the wiring inductance L5 is set to 20nH(s) and 400ns of values of the switching speed Toff of value 100A of the above-mentioned peak current Ip and the upper arm switching element T1 is used The electrical potential difference V (E0-N1) by which induction is carried out at the period of B of drawing 19 on both sides of the connection node E0 and the current detector 106 by the side of the emitter of the bottom arm switching element T2 between the connection nodes N1 of the opposite side of this connection node E0 is set to -5V by the following formula.

V(E0-N1) =-L5 and Ip/Toff=-{20-(E-9) -100}/{400- (E-9)}
=-5[V]

[0037] A current flows for the path from the connection node N1 to [with this electrical potential difference V (E0-N1) by which induction was carried out] the connection node E0 through the parasitism reactor of the wiring inductance value L7, reference diode 109, and the parasitism reactor of wiring inductance value L6. Supposing wiring inductance value L6 and L7 are equal here, induced voltage V (E0-N1) will take every [2 / 1/] between the negative side power supply terminal VSS and the connection node N1 and between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0. Therefore, the electrical potential difference V (VSS-N1) which

acts at the period of B of drawing 19 between the negative side power supply terminal VSS and the connection node N1 is set to -2.5V by the following formula.
V(VSS-N1)=V(E0-N1)/2=-2.5[V]
[0038] Moreover, the electrical potential difference V (E0-VS0) which acts between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0 is set to -2.5V by the following formula at the period of B of drawing 19 .
V(E0-VS0)=V(E0-N1)/2=-2.5[V]
[0039] In addition, in the period of B of drawing 19 , since especially an electrical potential difference is not built between the upper arm switching element driving signal criteria output terminal VS 1 and the connection node E1, the electrical potential difference V between them (VS1-E1) is 0V.
[0040] The electrical potential difference V (VS1-VS0) which acts among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides at the period of B of drawing 19 is set to -9.5V from the above-mentioned consideration from the following formula.
V(VS1-VS0)=V(VS1-E1)+V(E1-E0)+V(E0-VS0
=0-7-2.5=-9.5[V]
[0041] Thus, even if a wiring inductance is small, if a high current flows like the period of B of drawing 19 , the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing (-5V) among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides of the high proof pressure IC 100 will be carried out, and the high proof pressure IC 100 will cause proof-pressure destruction.
[0042] Other examples of the common single phase inverter equipment it was made to drive the arm switching element of the upper and lower sides of an inverter circuit with the high proof pressure IC are shown in drawing 20 . The single phase inverter circuit of this example is the thing of a configuration of being equivalent to the inverter part of the plane 1 of the three-phase-circuit inverter circuits shown in drawing 15 . That is, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.
[0043] And the emitter of the bottom arm switching element T2 is connected to the end of the current detector 106. The other end of the current detector 106 is connected to the negative electrode of DC power supply 108 through the external connection terminal N. The anode of diode D2 is connected to the negative side power supply terminal VSS of the high proof pressure IC 100. Common connection of the collector of the upper arm switching element T1 and the cathode of diode D1 is made, and they are connected to the external connection terminal P at the terminal by the side of forward (+) of DC power supply 108. A driving signal is inputted into each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2 from the high proof pressure IC 100, respectively.
[0044] In addition, about the configuration of others of an inverter circuit, the configuration of the high proof pressure IC 100, and connection between an inverter circuit and the high proof pressure IC 100, since it is the same as the thing of a configuration of being shown in drawing 18 , the explanation which attaches the same sign and overlaps is omitted.
[0045] the electrical potential difference V (E1-E0) built [like the example of a configuration of drawing 18 mentioned above also in the example of the configuration of this drawing 20] between the connection node E1 by the side of the emitter of the upper arm switching element T1, and the connection node E0 by the side of the emitter of the bottom arm switching element T2 with the electrical potential difference in which induction was carried out by the wiring inductance of ON state voltage VF of diode D2, or the chip of diode D2 and the bottom arm switching element T2 -- about -- it is set to -7V.
[0046] In addition, 400ns and the peak current Ip are set [the synthetic inductance value of the wiring inductances L1, L2, L3, and L4 / ON state voltage VF of 20nH(s) and diode D2] to 100A for the switching speed Toff of 2V and the upper arm switching element T1 like the consideration about the configuration of drawing 18 . However, in the example of this drawing 20 , since the current which flows diode D2 does not pass along the current detector 106, between the connection node E0 and the

bottom arm switching element driving signal criteria output terminal VS 0, an electrical potential difference does not generate it.

[0047] Therefore, the electrical potential difference of V (E1-E0) is built as it is between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0. That is, between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, the seal of approval of the electrical potential difference (-7V) which is less than (-5V) will be carried out in the minimum range of rated pressure-proofing, and the high proof pressure IC 100 will cause proof-pressure destruction.

[0048] Moreover, at the moment of the current which was flowing to the bottom arm switching element T2 being intercepted, an electrical potential difference occurs with the parasitism reactor of the wiring inductance value L5 which is parasitic between the connection node E0 and the current detector 106, and the partial pressure of the generated electrical potential difference is carried out to wiring inductance value L6 and each parasitism reactor of L7.

[0049] Therefore, an electrical potential difference V (E0-VS0) occurs between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0. Like the consideration about the configuration of drawing 18 , if the wiring inductance L5 is set to 20nH(s) and switching speed Toff of 100A and the upper arm switching element T1 is set to 400ns for the peak current Ip, V (E0-VS0) will turn into -2.5V.

[0050] Among the connection nodes E1 and E0, an electrical potential difference V (E1-E0) occurs with the parasitism reactor of the wiring inductance value L1, the reactor, and ON state voltage Vce of a switching element T2 of the synthetic inductance value L8 which is parasitic on the circuit pattern of the bottom arm switching element T2. In the synthetic inductance value of L1 and L8, if 20nH(s) and said Vce are set to 2V and switching speed Toff of 100A and the upper arm switching element T1 is set to 400ns for the peak current Ip, the value of an electrical potential difference V (E1-E0) will be set to -3V from the following formula.

V(E1-E0)=-(L1+L8)
- Ip/Toff+Vce =-{20 -(E-9)- 100}
/{400- (E-9)} +2 = -3 [V]

[0051] In addition, since especially an electrical potential difference is not built between the upper arm switching element driving signal criteria output terminal VS 1 and the connection node E1, the electrical potential difference V between them (VS1-E1) is 0V.

[0052] The electrical potential difference V (VS1-VS0) which acts among the up-and-down arm switching element driving signal criteria output terminals VS1 and VS0 is set to -5.5V from the above-mentioned consideration from the following formula.

V(VS1-VS0)=V(VS1-E1
+V(E1-E0)
+V(E0-VS0)
=0-3-2.5=-5.5[V]

[0053] Thus, also in the equipment of a configuration of being shown in drawing 20 , if a high current flows, the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing (-5V) among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides of the high proof pressure IC 100 will be carried out, and the high proof pressure IC 100 will cause proof-pressure destruction.

[0054] Although the value of an electrical potential difference V (VS1-VS0) changes with methods of arrangement [consideration / about the equipment of a configuration of being shown in above-mentioned drawing 18 and drawing 20 , respectively / above-mentioned] of the current detector 106 Under the effect by few inductances of wiring of a chip, or few inductances of wiring of the current detector 106 It turns out that the minus electrical potential difference which is less than the minimum value of rated pressure-proofing among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides to the case of a high current drive may occur.

[0055] About the consideration mentioned above, the minus electrical potential difference which is the same when not forming a current detector (i.e., also when not performing current detection), as shown in drawing 21 , and is less than the minimum value of rated pressure-proofing with few inductances of wiring of a chip among the up-and-down arm switching element driving signal criteria output terminals VS1 and VS0 in a high current drive may occur. Therefore, the high proof pressure IC 100 will cause proof-pressure destruction. In addition, reference diode 109 is not formed with the inverter equipment of a configuration of being shown in drawing 21 .

[0056] The common three-phase-circuit inverter equipment it was made to drive the arm switching element of three pairs of upper and lower sides of an inverter circuit with the high proof pressure IC is shown in drawing 22 . The three-phase-circuit inverter circuit of this example is the thing of a configuration of being equivalent to the three-phase-circuit inverter circuit shown in drawing 17 . That is, in eye the 1st phase, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.

[0057] In eye the 2nd phase, antiparallel connection of the up-and-down diodes D3 and D4 is carried out to switching element T3 of the pair to which it comes to connect the emitter of upper arm switching element T3, and the collector of bottom arm switching element T four, and T four, respectively. In eye the 3rd phase, antiparallel connection of the up-and-down diodes D5 and D6 is carried out to the switching elements T5 and T6 of a pair with which it comes to connect the emitter of the upper arm switching element T5, and the collector of the bottom arm switching element T6, respectively.

[0058] And common connection of the anode of the diodes D2, D4, and D6 by which antiparallel connection was carried out to each Shimo arm switching element T2, T four, the emitter of T6, and them is made, and common connection is made at the end of the current detector 214. The other end of the current detector 214 is connected to the external connection terminal N. Common connection of the cathode of the diodes D1, D3, and D5 by which antiparallel connection was carried out to each up arm switching element T1, T3, the collector of T5, and them is made at the external connection terminal P. A driving signal is inputted into each up arm switching element T1, T3, the gate G1 of T5, G3, G5 and each Shimo arm switching element T2, T four, and the gates G2, G4, and G6 of T6 from the high proof pressure IC 200, respectively.

[0059] Moreover, three external connection terminals U, V, and W are formed in the inverter circuit of the above-mentioned configuration in addition to the above-mentioned external connection terminals P and N. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1 of eye the 1st phase. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1 of eye the 1st phase. The external connection terminal V is connected to the connection node E2 by the side of the emitter of upper arm switching element T3 of eye the 2nd phase. The external connection terminal W is connected to the connection node E3 by the side of the emitter of the upper arm switching element T5 of eye the 3rd phase.

[0060] Although not illustrated especially, a parasitism reactor exists in each Shimo arm switching element T2, T four, the wiring section of T6, and the wiring section of each diodes D2, D4, and D6, respectively. Moreover, a parasitism reactor exists also in wiring between the connection node E0 by the side of each Shimo arm switching element T2, T four, and the emitter of T6, and the connection node N1 prepared in the opposite side (namely, between the current detector 214 and the external connection terminals N) of E0 on both sides of the current detector 214.

[0061] The high proof pressure IC 200 The driving signal input terminals UPi, UNi, VPi, VNi, WPi, and WNi of this IC200 are minded. The signal inputted from the outside Each output signal of three level shifters b2, b3, and b4 and level shifters b2, b3, and b4 which generates the signal of the input buffer b1 held temporarily and the floating potential which received the output signal of the input buffer b1, and floated from the potential of the signal It receives and three signals outputted from the upper arm switching element T1, T3, the three upper arm side driver circuits b5, b6, and b7 that drive T5, and an input buffer b1, respectively are received., respectively the bottom arm switching element T2, T four,

and T6 It has the bottom arm side driver circuits b8, b9, and b10 to drive, the overcurrent detector b11 which performs detection of an overcurrent, and the error signal generator b12 which receives the detecting signal outputted from the overcurrent detector b11, and generates an error signal.
[0062] Each up arm side driver circuits b5, b6, and b7 output a driving signal to each up arm switching element T1, T3, and T5 through the upper arm switching element driving signal output terminals UPo, VPo, and WPo prepared in the high proof pressure IC 200, respectively. Moreover, a forward and negative floating electrical potential difference is impressed to the high proof pressure IC 200 from the outside in each up arm side driver circuits b5, b6, and b7 through the floating power-source forward side input terminals VB1, VB2, and VB3 and the floating power-source negative side input terminals VS1, VS2, and VS3 which were prepared, respectively. Each floating power-source negative side input terminals VS1, VS2, and VS3 serve as each up arm switching element T1, T3, and the upper arm switching element driving signal criteria output terminal of T5, respectively.
[0063] Each Shimo arm side driver circuits b8, b9, and b10 output a driving signal to each Shimo arm switching element T2, T four, and T6 through the bottom arm switching element driving signal output terminals UNo, VNo, and WNo prepared in the high proof pressure IC 200, respectively. Moreover, forward supply voltage is impressed to each Shimo arm side driver circuits b8, b9, and b10 from the outside through the forward side power supply terminal VCC prepared in the high proof pressure IC 200. Common connection of each Shimo arm side driver circuits b8, b9, and b10 is made at the bottom arm switching element driving signal criteria output terminal VS 0 prepared in the high proof pressure IC 200.
[0064] The overcurrent detector b11 is connected to the current detection terminal OC prepared in the high proof pressure IC 200.
[0065] The error signal generator b12 outputs an error signal to a control unit, an alarm information means, etc. which the exterior does not illustrate through the error output terminal Fo prepared in the high proof pressure IC 200.
[0066] The forward side power supply terminal VCC and the negative side power supply terminal VSS which were prepared in the high proof pressure IC 200, respectively are connected to the positive electrode and negative electrode of an external power 201, respectively. And the negative side power supply terminal VSS is grounded.
[0067] External [of the capacitor 205,206,207 of three diodes / 202,203,204 of 3 / and reference diode 215 other than the above-mentioned external power 201] is carried out to the high proof pressure IC 200. Namely, common connection of each anode is made at the forward side power supply terminal VCC, and, as for diode 202,203,204, each cathode is connected to the floating power-source forward side input terminals VB1, VB2, and VB3, respectively. The capacitor 205 is connected between the floating power-source forward side input terminal VB 1 and the floating power-source negative side input terminal VS 1.
[0068] The capacitor 206 is connected between the floating power-source forward side input terminal VB 2 and the floating power-source negative side input terminal VS 2. The capacitor 207 is connected between the floating power-source forward side input terminal VB 3 and the floating power-source negative side input terminal VS 3. Reference diode 215 is formed in the overvoltage protections of the bottom arm switching element driving signal criteria output terminal VS 0, and is connected between the bottom arm switching element driving signal criteria output terminal VS 0 and the negative side power supply terminal VSS.
[0069] The high proof pressure IC 200 is connected to the inverter circuit of the above-mentioned three phase circuit as follows. That is, three floating power-source negative side input terminals (upper arm switching element driving signal criteria output terminal) VS1, VS2, and VS3 of the high proof pressure IC 200 are connected to each connection nodes E1, E2, and E3 by the side of the upper arm switching element T1, T3, and the emitter of T5, respectively.
[0070] The three upper arm switching element driving signal output terminals UPo, VPo, and WPo are connected to the upper arm switching element T1, T3, each gate G1 of T5, G3, and G5 through gate resistance 208,209,210, respectively. The bottom arm switching element driving signal criteria output

terminal VS 0 is connected to the connection node E0 by the side of the bottom arm switching element T2, T four, and the emitter of T6.

[0071] The bottom arm switching element driving signal output terminals UNo, VNo, and WNo of three pieces are connected to each gates G2, G4, and G6 of the bottom arm switching element T2, T four, and T6 through gate resistance 211,212,213, respectively. The current detection terminal OC is connected to said connection node E0.

[0072] Moreover, the negative side power supply terminal VSS is connected to said connection node N1 of an inverter circuit. Since the current detector 214 is between these connection node E0 and the connection node N1 as mentioned above, the detection electrical potential difference of the current detector 214 will be impressed to the current detection terminal OC.

[0073] Although not illustrated, the parasitism reactor exists in wiring between the bottom arm switching element driving signal criteria output terminal VS 0 and the connection node E0, and especially wiring between the negative side power supply terminal VSS and the connection node N1, respectively.

[0074] Also in the inverter equipment of a three phase circuit shown in drawing 22 , like the case of the single phase inverter equipment shown in drawing 18 , if a high current flows, the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing, respectively between the up-and-down arm switching element driving signal criteria output terminal VS 1, VS0 and VS2, and VS0, VS3 and VS0 will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction.

[0075] Other examples of the common three-phase-circuit inverter equipment it was made to drive the arm switching element of three pairs of upper and lower sides of an inverter circuit with the high proof pressure IC are shown in drawing 23 . The three-phase-circuit inverter circuit of this example is the thing of a configuration of being equivalent to the three-phase-circuit inverter circuit shown in drawing 15 . That is, in eye the 1st phase, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.

[0076] In eye the 2nd phase, antiparallel connection of the up-and-down diodes D3 and D4 is carried out to switching element T3 of the pair to which it comes to connect the emitter of upper arm switching element T3, and the collector of bottom arm switching element T four, and T four, respectively. In eye the 3rd phase, antiparallel connection of the up-and-down diodes D5 and D6 is carried out to the switching elements T5 and T6 of a pair with which it comes to connect the emitter of the upper arm switching element T5, and the collector of the bottom arm switching element T6, respectively.

[0077] And each Shimo arm switching element T2, T four, and the emitter of T6 are connected to the end of the current detector 214. The other end of the current detector 214 is connected to the external connection terminal N. The anode of each diodes D2, D4, and D6 is connected to the negative side power supply terminal VSS of the high proof pressure IC 200. Common connection of each up arm switching element T1, T3, the collector of T5, and the cathode of each diodes D1, D3, and D5 is made at the external connection terminal P. A driving signal is inputted into each up arm switching element T1, T3, the gate G1 of T5, G3, G5 and each Shimo arm switching element T2, T four, and the gates G2, G4, and G6 of T6 from the high proof pressure IC 200, respectively.

[0078] In addition, about the configuration of others of a three-phase-circuit inverter circuit, the configuration of the high proof pressure IC 200, and connection between an inverter circuit and the high proof pressure IC 200, since it is the same as the thing of a configuration of being shown in drawing 22 , the explanation which attaches the same sign and overlaps is omitted.

[0079] Since the current which flows diodes D2, D4, and D6 does not pass along the current detector 214 by the example of the configuration of this drawing 23 , Although an electrical potential difference does not occur between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0 The seal of approval of the electrical potential difference which is still less than the minimum range of rated pressure-proofing, respectively between the arm switching element

driving signal criteria output terminal VS 1 of the upper and lower sides to the case of a high current drive, VS0 and VS2, and VS0, VS3 and VS0 will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction.

[0080] Moreover, as shown in drawing 24 , the same is said of the case where a current detector is not formed, and the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing, respectively between the up-and-down arm switching element driving signal criteria output terminal VS 1, VS0 and VS2, and VS0, VS3 and VS0 in a high current drive will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction. In addition, reference diode 215 is not formed with the inverter equipment of a configuration of being shown in drawing 24 .

[0081]

[Problem(s) to be Solved by the Invention] As mentioned above, with the single phase and the three-phase-circuit inverter equipment which used the conventional high proof pressure IC 100,200 for a switching element drive, there was a trouble that the electrical potential difference exceeding the rated voltage might be built over the high proof pressure IC 100,200, and the high proof pressure IC 100,200 might break by part for few [the bottom arm switching element T2, T four, T6 or diodes D2, D4, and D6, the connection pattern of the current detector 106,214, etc.] inductances at the time of a high current drive.

[0082] This invention was made in order to solve the above-mentioned trouble, and it aims at obtaining the inverter equipment which can prevent the high proof pressure IC for a switching element drive breaking at the time of a high current drive.

[0083]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the inverter equipment concerning this invention connects a clamp diode between the upper arm switching element driving signal criteria output terminal of the high proof pressure IC which drives the switching element of the upper and lower sides of a single phase inverter circuit, and a bottom arm switching element driving signal criteria output terminal.

[0084] According to the inverter equipment concerning this invention, in single phase inverter equipment, the negative electrical potential difference impressed between the upper arm switching element driving signal criteria output terminal of the high proof pressure IC and the bottom arm switching element driving signal criteria output terminal can prevent that it is less than the rated proof-pressure minimum value between those terminals.

[0085] The inverter equipment concerning the next invention connects a clamp diode, respectively between three upper arm switching element driving signal criteria output terminals of the high proof pressure IC which drive the switching element of the upper and lower sides of a three-phase-circuit inverter circuit, and bottom arm switching element driving signal criteria output terminals.

[0086] According to the inverter equipment concerning this invention, in three-phase-circuit inverter equipment, the negative electrical potential difference impressed, respectively between three upper arm switching element driving signal criteria output terminals of the high proof pressure IC and bottom arm switching element driving signal criteria output terminals can prevent that it is less than the rated proof-pressure minimum value between those terminals.

[0087] The inverter equipment concerning the next invention uses a clamp diode as the external components of the high proof pressure IC.

[0088] According to the inverter equipment concerning this invention, while the design change of the high proof pressure IC is unnecessary, this invention is applicable also to the inverter equipment which used the existing high proof pressure IC.

[0089] The inverter equipment concerning the next invention forms the means of communication which transmits the signal which operates according to the independent power source other than the drive power source of the high proof pressure IC which drives the switching element of the upper and lower sides of the inverter circuit which has a current detection means, and is outputted from a current detection means to the high proof pressure IC.

[0090] Since potential of a negative side power supply terminal and a bottom arm switching element driving signal criteria output terminal can be made equal by having established a means to transmit the output from a current detector to the high proof pressure IC according to the inverter equipment concerning this invention, it is prevented that a negative electrical potential difference is impressed with the circuit pattern of a current detector etc. between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.
[0091] The inverter equipment concerning the next invention constitutes a means of communication with an operational amplifier, and uses it as the external components of the high proof pressure IC.
[0092] According to the inverter equipment concerning this invention, while the design change of the high proof pressure IC is unnecessary, this invention is applicable also to the inverter equipment which used the existing high proof pressure IC.
[0093] The inverter equipment concerning the next invention connects to the anode of the diode of a bottom arm wiring connected to the bottom arm switching element driving signal criteria output terminal while connecting wiring connected to the upper arm switching element driving signal criteria output terminal of the high proof pressure IC which drives the switching element of the upper and lower sides of a single phase inverter circuit near the cathode of the diode of a bottom arm.
[0094] In not forming a current detector according to the inverter equipment concerning this invention It is lost by the amount of [by the inductance produced with the conventional circuit pattern] electrical-potential-difference generating. Since the negative electrical potential difference which may be impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal turns into only ON state voltage of the diode of a bottom arm mostly It is prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal. If the negative electrical potential difference generated by the current detector between up-and-down arm switching element driving signal criteria output terminals is low when a current detector is formed, it will be prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.
[0095] The inverter equipment concerning the next invention prepares the bonding pad of dedication by which the other end of wiring by which the end was connected to the bottom arm switching element driving signal criteria output terminal was connected to the three-phase-circuit inverter circuit part. The high proof pressure IC which drives the switching element of the upper and lower sides of a three-phase-circuit inverter circuit While connecting three wiring connected to three upper arm switching element driving signal criteria output terminals, respectively near the cathode of the diode of the bottom arm of three, respectively The bonding pad of said dedication and the anode of the diode of the bottom arm of three are electrically connected with a wire, respectively.
[0096] According to the inverter equipment concerning this invention, it sets to three-phase-circuit inverter equipment. While the current which becomes main for each wiring path which results in each up arm switching element driving signal criteria output terminal of the high proof pressure IC from each cathode of 3 diodes of a bottom arm flows Since the current which becomes main also for each wiring path which results in each Shimo arm switching element driving signal criteria output terminal of the high proof pressure IC from each anode of three diodes of a bottom arm flows Since the negative electrical potential difference which may be impressed between three upper arm switching element driving signal criteria output terminals and bottom arm switching element driving signal criteria output terminals turns into only ON state voltage of the diode of the bottom arm of about three, respectively in not forming a current detector It is prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between three upper arm switching element driving signal criteria output terminals and bottom arm switching element driving signal criteria output terminals. If each negative electrical potential difference generated by the current detector between up-and-down arm switching element driving signal criteria output terminals is low when a current detector

is formed, it will be prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.

[0097] The diode with larger current capacity as diode of the bottom arm of the inverter circuit driven with the high proof pressure IC than the diode of other switching elements and an upper arm is used for the inverter equipment concerning the next invention.

[0098] Since the ON state voltage of the diode of the bottom arm which is one of the causes of destructive of the high proof pressure IC when only the diode of a bottom arm uses what has large current capacity can be stopped low according to the inverter equipment concerning this invention, the margin to proof-pressure destruction of the high proof pressure IC becomes so large.

[0099]

[Embodiment of the Invention]

(Gestalt 1 of operation) Drawing 1 is the schematic diagram showing an example of the single phase inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 1 of this operation to drawing 18 A clamp diode 110 is connected between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Only when the electrical potential difference V between the criteria output terminals VS [VS1 and] 0 of these upper and lower sides (VS1-VS0) turns into a negative electrical potential difference, a clamp diode 110 turns on and the electrical potential difference V (VS1-VS0) is maintained at the ON state voltage of a clamp diode 110.

[0100] In drawing 1 T1 and T2, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1 and D2 was carried out to the upper arm switching element T1 and the bottom arm switching element T2, respectively, G1 and G2, respectively The gate of the upper arm switching element T1 and the bottom arm switching element T2, The resistance to which 104 and 105 were connected to each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2, respectively, They are the DC power supply which a current detector becomes in 106 and the reactor as a load and 108 become from power-source body 108a and capacitor 108b in 107.

[0101] E1 and E0 Moreover, the connection node by the side of each emitter of the upper arm switching element T1 and the bottom arm switching element T2, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, The reactor with which the output terminal of an inverter circuit, L1, L2, L3, L4 and L5, L6, and L7 are [U] parasitic on a wiring part, and I1, I2 and I3 are the current which flows the upper arm switching element T1, the current which flows to diode D2, and a current which flows a reactor 107, respectively. The current detector 106 is formed on the bus-bar with which common connection of the emitter of the bottom arm switching element T2 and the anode of diode D2 was made.

[0102] In drawing 1 100 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 101 supplies driver voltage to the high proof pressure IC 100, and 102 Diode, As for a capacitor and 109, reference diode, and a1, a2, a3, a4, a5 and a6 is [103] the circuit blocks inside the high proof pressure IC 100. As for the bottom arm side driver circuit where the upper arm side driver circuit where an input buffer and a2 drive a level shifter, and, as for a3, a1 drives the upper arm switching element T1, and a4 drive the bottom arm switching element T2, and a5, an overcurrent detector and a6 are error signal generators.

[0103] Moreover, UPi, UNi, UPo, UNo, VB1, VS1, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 100. The upper arm switching element driving signal output terminal to which UPi and UNi output a driving signal input terminal, and UPo outputs the driving signal of the upper arm switching element T1, respectively, The bottom arm switching element driving signal output terminal to which UNo outputs the driving signal of the bottom arm switching element T2, While VB1 is a floating power-source forward side input terminal and VS1 is a floating power-source

negative side input terminal, an upper arm switching element driving signal criteria output terminal, For VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.

[0104] In the configuration of the inverter equipment shown in drawing 1 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 18 .

[0105] By the way, generally the minimum value of pressure-proofing of the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent. That is, the rated proof-pressure minimum value of the electrical potential difference V between the arm switching element driving signal criteria output terminals VS [VS1 and] 0 of the upper and lower sides of the high proof pressure IC 100 (VS1-VS0) is abbreviation-5V.

[0106] Therefore, especially in the gestalt 1 of this operation, as said clamp diode 110, although not limited, the common diode whose ON state voltage is about 0.7V-2V, for example is used. Then, when a negative electrical potential difference is built between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, the electrical potential difference between them is clamped by the ON state voltage of a clamp diode 110, i.e., about -0.7V--2V. In addition, it is good to form a clamp diode 110 immediately near the criteria output terminals VS0 and VS1 of the high proof pressure IC 100 preferably, and to stop as short as possible the wire length from these terminals VS0 and VS1 to a clamp diode 110.

[0107] An operation of the inverter equipment of a configuration of being shown in drawing 1 is explained. Only when the seal of approval of the negative electrical potential difference which can become the cause of making this IC100 destroying between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 is carried out, a clamp diode 110 serves as ON and clamps the electrical potential difference V between these terminals VS [VS1 and] 0 (VS1-VS0) to ON state voltage (about 0.7V-2V). Therefore, an electrical potential difference V (VS1-VS0) becomes about -0.7V--2V, and is not less than rated proof-pressure minimum value-5V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100.

[0108] As explained above, according to the gestalt 1 of this operation The electrical potential difference V between terminals (VS1-VS0) when a negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 becomes about -0.7V--2V. Since it can prevent that it is less than rated proof-pressure minimum value-5V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0109] In addition, the anode of diode D2 is connected to the direct negative side power supply terminal VSS like the single phase inverter equipment shown in drawing 2 , without minding the current detector 106. Also in the inverter equipment of a configuration of that only the emitter of the bottom arm switching element T2 is shown in drawing 20 linked to the current detector 106 A clamp diode 110 can be formed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential difference V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100 (VS1-VS0) is less than rated proof-pressure minimum value-5V, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0110] Moreover, also in the inverter equipment of a configuration of being shown in drawing 21 it was made not to form a current detector like the single phase inverter equipment shown in drawing 3 , a clamp diode 110 can be formed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential difference V

between these terminals VS [VS1 and] 0 of the high proof pressure IC 100 (VS1-VS0) is less than rated proof-pressure minimum value-5V, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0111] (Gestalt 2 of operation) Drawing 4 is the schematic diagram showing an example of the three-phase-circuit inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 2 of this operation to drawing 22 Between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminals VS 0, Between the upper arm switching element driving signal criteria output terminal VS 2 and the bottom arm switching element driving signal criteria output terminals VS 0, A clamp diode 216,217,218 is connected, respectively between the upper arm switching element driving signal criteria output terminal VS 3 and the bottom arm switching element driving signal criteria output terminal VS 0.

[0112] And each electrical potential difference V between each upper criteria output terminals VS1, VS2, and VS3 and the lower criteria output terminal VS 0 (VS1-VS0) Only when V (VS2-VS0) and V (VS3-VS0) become a negative electrical potential difference, respectively, the clamp diode 216,217,218 turns on. Each electrical potential difference V (VS1-VS0) V (VS2-VS0) and V (VS3-VS0) are maintained at the ON state voltage of a clamp diode 216,217,218, respectively.

[0113] In drawing 4 T1, T3, T5 and T2, T four, and T6, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1, D3, D5, and D2, D4 and D6 was carried out to the upper arm switching element T1, T3, T5 and the bottom arm switching element T2, T four, and T6, respectively, G1, G3, G5, and G2, G4 and G6 are the upper arm switching element T1, T3, T5 and the bottom arm switching element T2, T four, and the gate of T6, respectively.

[0114] The resistance by which 208,209,210 and 211,212,213 were connected to the upper arm switching element T1, T3, the gate G1 of T5, G3, G5 and the bottom arm switching element T2, T four, and the gates G2, G4, and G6 of T6, respectively, and 214 Moreover, a current detector, E1, E2, and E3, respectively The upper arm switching element T1, T3, the connection node by the side of the emitter of T5, The connection node the bottom arm switching element T2, T four, and by the side of each emitter of T6 with common E0, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, and U, V and W are the output terminals of the inverter circuit of each three phase circuit, respectively. The current detector 214 is formed on each Shimo arm switching element T2, T four, and the bus-bar with which common connection of the emitter of T6 and the anode of each diodes D2, D4, and D6 was made.

[0115] In drawing 4 200 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 201 supplies driver voltage to the high proof pressure IC 200, and 202,203,204 Diode, A capacitor and 215 205,206,207 Reference diode, b1, b2, b3, b4, b5, b6, b7, b8, b9, b10, b11, and b12 are the circuit blocks inside the high proof pressure IC 200. The upper arm side driver circuit where an input buffer, and b2, b3 and b4 drive a level shifter, and, as for b5, b6, and b7, b1 drives the upper arm switching element T1, T3, and T5, respectively, As for the bottom arm side driver circuit where b8, b9, and b10 drive the bottom arm switching element T2, T four, and T6, respectively, and b11, an overcurrent detector and b12 are error signal generators.

[0116] Moreover, UPi, UNi, VPi, VNi, WPi, WNi, UPo, VPo, WPo, UNo, VNo, WNo, VB1, VB2, VB3, VS1, VS2, VS3, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 200. UPi, VPi, WPi, and UNi, VNi and WNi, respectively A driving signal input terminal, The upper arm switching element driving signal output terminal to which UPo, VPo, and WPo output the upper arm switching element T1, T3, and the driving signal of T5, respectively, The bottom arm switching element driving signal output terminal to which UNo, VNo, and WNo output the bottom arm switching element T2, T four, and the driving signal of T6, respectively, While VB1, VB2, and VB3 are floating power-source negative side input terminals, a floating power-source forward side input terminal, and VS1, VS2 and VS3 An upper arm switching element driving signal criteria output terminal, For

VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.
[0117] In the configuration of the inverter equipment shown in drawing 4 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 22 .
[0118] Here, generally the minimum value of each pressure-proofing of the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent as the gestalt 1 of operation explained. That is, the rated proof-pressure minimum value of the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 and the bottom arm switching element driving signal criteria output terminal VS 0 is abbreviation-5V, respectively.
 [0119] Therefore, especially in the gestalt 2 of this operation, as said clamp diode 216,217,218, although not limited, the common diode whose ON state voltage is about 0.7V-2V, for example is used. Then, when a negative electrical potential difference is built between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 and the bottom arm switching element driving signal criteria output terminal VS 0, the electrical potential difference between them is clamped by the ON state voltage of a clamp diode 216,217,218, i.e., about -0.7V--2V.
[0120] In addition, it is good to form each clamp diode 216,217,218 immediately the criteria output terminal VS 0 of the high proof pressure IC 200, and near VS1, VS2, and VS3 preferably, and to stop as short as possible these terminals VS 0 and the wire length from VS1, VS2, and VS3 to each clamp diode 216,217,218.
[0121] An operation of the inverter equipment of a configuration of being shown in drawing 4 is explained. Between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 Only when the seal of approval of the negative electrical potential difference which can become the cause of making this IC200 destroying is carried out A clamp diode 216,217,218 serves as ON and clamps the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS1, VS2, VS3, and VS0 to ON state voltage (about 0.7V-2V), respectively. Therefore, electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) become about -0.7V--2V, respectively, and are not less than rated proof-pressure minimum value-5V between these terminals VS1, VS2, VS3, and VS0 of the high proof pressure IC 200.
[0122] As explained above, according to the gestalt 2 of this operation The electrical potential difference V between terminals when a negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 (VS1-VS0) Since it can prevent that V (VS2-VS0) and V (VS3-VS0) become about -0.7V--2V, respectively, and it is less than rated proof-pressure minimum value-5V between these terminals VS1, VS2, VS3, and VS0 of the high proof pressure IC 200 Proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0123] In addition, the anode of each diodes D2, D4, and D6 is connected to the direct negative side power supply terminal VSS like the three-phase-circuit inverter equipment shown in drawing 5 , without minding the current detector 214. Also in each Shimo arm switching element T2, T four, and the inverter equipment of a configuration of that only the emitter of T6 is shown in drawing 23 linked to the current detector 214 A clamp diode 216,217,218 can be formed, respectively between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS [VS1 VS2, VS3, and] 0 of the high proof pressure IC 200 are less than rated proof-pressure minimum value-5V, respectively, proof-pressure destruction of the high proof pressure IC 200

can be prevented.
[0124] Moreover, also in the inverter equipment of a configuration of being shown in drawing 24 it was made not to form a current detector like the three-phase-circuit inverter equipment shown in drawing 6 , a clamp diode 216,217,218 can be formed, respectively between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS [VS1 VS2, VS3, and] 0 of the high proof pressure IC 200 are less than rated proof-pressure minimum value-5V, respectively, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0125] (Gestalt 3 of operation) Drawing 7 is the schematic diagram showing an example of the single phase inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 3 of this operation to drawing 18 Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 106 to the high proof pressure IC 100 is formed..By connecting the negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0, and making it same electric potential It prevents building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0.
[0126] In drawing 7 T1 and T2, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1 and D2 was carried out to the upper arm switching element T1 and the bottom arm switching element T2, respectively, G1 and G2, respectively The gate of the upper arm switching element T1 and the bottom arm switching element T2, The resistance to which 104 and 105 were connected to each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2, respectively, They are the DC power supply which a current detector becomes in 106 and the reactor as a load and 108 become from power-source body 108a and capacitor 108b in 107.
[0127] E1 and E0 Moreover, the connection node by the side of each emitter of the upper arm switching element T1 and the bottom arm switching element T2, N1 sandwiches the current detector 106. With the connection node E0 The connection node of the opposite side, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, The reactor with which the output terminal of an inverter circuit, L1, L2, L3, L4 and L5, and L6 are [U] parasitic on a wiring part, and I1, I2 and I3 are the current which flows the upper arm switching element T1, the current which flows to diode D2, and a current which flows a reactor 107, respectively. The current detector 106 is formed on the bus-bar with which common connection of the emitter of the bottom arm switching element T2 and the anode of diode D2 was made.
[0128] In drawing 7 100 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 101 supplies driver voltage to the high proof pressure IC 100, and 102 Diode, 103 is a capacitor and a1, a2, a3, a4, a5, and a6 are the circuit blocks inside the high proof pressure IC 100. As for the bottom arm side driver circuit where the upper arm side driver circuit where an input buffer and a2 drive a level shifter, and, as for a3, a1 drives the upper arm switching element T1, and a4 drive the bottom arm switching element T2, and a5, an overcurrent detector and a6 are error signal generators.
[0129] Moreover, UPi, UNi, UPo, UNo, VB1, VS1, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 100. The upper arm switching element driving signal output terminal to which UPi and UNi output a driving signal input terminal, and UPo outputs the driving signal of the upper arm switching element T1, respectively, The bottom arm switching element driving signal output terminal to which UNo outputs the driving signal of the bottom arm switching element T2, While VB1 is a floating power-source forward side input terminal and VS1 is a floating power-source

negative side input terminal, an upper arm switching element driving signal criteria output terminal, For VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.

[0130] In the configuration of the inverter equipment shown in drawing 7 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 18 .

[0131] The operational amplifier 111 has negative supply with the another high proof pressure IC 100, the forward side input terminal is connected to the connection node E0 near the emitter of the bottom arm switching element T2, and the negative side input terminal is connected to the connection node N1. The output terminal of an operational amplifier 111 is connected to the overcurrent detector a5 through the current detection terminal OC of the high proof pressure IC 100.

[0132] The anode of the clamp diode 114 which prevents building a negative electrical potential difference over this terminal OC is connected to the current detection terminal OC. The cathode of the clamp diode 114 is connected to the grounding point. In addition, since a clamp diode 114 only clamps the output of an operational amplifier 111, it is good for the diode for small signals.

[0133] Preferably, it is good to connect the negative side power supply terminal VSS of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0 immediately near the high proof pressure IC 100.

[0134] An operation of the inverter equipment of a configuration of being shown in drawing 7 is explained. Usually, since the potential difference to which the polar electrical-potential-difference E0, i.e., connection node, side as shown in the current detector 106 by "+" and "-" at drawing 7 becomes higher than the connection node N1 side occurs, it is reversed with an operational amplifier 111 and a forward electrical potential difference is impressed to the current detection terminal OC. Since the operational amplifier 111 has the negative electrical potential difference when a current is intercepted and induction of the negative electrical potential difference is carried out by few wiring inductances, as explained in the above-mentioned conventional technique, if it is electrical-potential-difference within the limits of the negative electrical potential difference, an operational amplifier 111 will not break. Although the negative electrical potential difference outputted from the operational amplifier 111 will be impressed to the current detection terminal OC of the high proof pressure IC in that case, since the potential of the current detection terminal OC is clamped by the clamp diode 114, the high proof pressure IC 100 does not destroy it.

[0135] By having established a means to transmit the output from the current detector 106 to the high proof pressure IC 100 according to the gestalt 3 of this operation, as explained above Since potential of the negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 can be made equal It can prevent impressing a negative electrical potential difference with the circuit pattern of the current detector 106 etc. between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, and proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0136] In addition, like the single phase inverter equipment shown in drawing 8 , as the current detector 106 is not minded for the anode of diode D2, only the emitter of the bottom arm switching element T2 is also set to the inverter equipment of a configuration of being shown in drawing 20 linked to the current detector 106. Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 106 to the high proof pressure IC 100 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 100

can be prevented.
[0137] Moreover, it also sets to the inverter equipment of a configuration of being shown in drawing 22 which comes to prepare the current detector 214 like the three-phase-circuit inverter equipment shown in drawing 9 on each Shimo arm switching element T2, T four, and the bus-bar with which common connection of the emitter of T6 and the anode of each diodes D2, D4, and D6 was made. Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 214 to the high proof pressure IC 200 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential.
[0138] Moreover, for the current detection terminal OC, it clamps with a clamp diode 114. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0139] Furthermore, the ** which does not connect the anode of each diodes D2, D4, and D6 to the current detector 214 like the three-phase-circuit inverter equipment shown in drawing 10 , Also in each Shimo arm switching element T2, T four, and the inverter equipment of a configuration of that only the emitter of T6 is shown in drawing 23 which it comes to connect with the current detector 214 Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 214 to the high proof pressure IC 200 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential.
[0140] Moreover, for the current detection terminal OC, it clamps with a clamp diode 114. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0141] Although the operational amplifier 111 was used with the gestalt 3 of the above-mentioned implementation further again as a means to transmit the output of the current detector 106,214 to the high proof pressure IC 100,200, the same effectiveness is acquired, even if it replaces with an operational amplifier 111 and uses insulating amplifier, an analog photo coupler, etc.
[0142] (Gestalt 4 of operation) Drawing 11 is the mimetic diagram showing the example of chip arrangement of the inverter circuit in the single phase inverter equipment concerning this invention. This inverter circuit The chip of the upper arm switching element T1 The chip of diode D1 by which antiparallel connection was carried out to 301 and the upper arm switching element T1 (An upper arm switching element chip is called hereafter) The chip of 302 and the bottom arm switching element T2 (An upper arm diode chip is called hereafter) The chip of diode D2 by which antiparallel connection was carried out to 303 and the bottom arm switching element T2 (A bottom arm switching element chip is called hereafter) The bonding pad used as the power supply terminal P which impresses forward supply voltage to 304 and an inverter circuit (A bottom arm diode chip is called hereafter) (In the gestalt 4 of this operation, it considers as a bonding pad P hereafter) It has composition equipped with the bonding pad (it considers as a bonding pad N similarly hereafter) used as the power supply terminal N which impresses negative supply voltage to an inverter circuit, and the bonding pad (it considers as a bonding pad U similarly hereafter) used as the output terminal U of an inverter circuit.
[0143] Gate 301G (field surrounded squarely) are prepared in a part of the front face, and the upper arm switching element chip 301 is formed so that chip front faces other than the field which is gate 301G may serve as collector 301C. The rear face of the upper arm switching element chip 301 is emitter 301E. Collector 301C of the upper arm switching element T1 is directly in contact with the bonding pad P.
[0144] Emitter 301E of the upper arm switching element T1 is electrically connected to the bonding pad U through the wire W1. Although not limited especially, in drawing 11 , the wire W1 serves as a wire bundle which consists of three wires. Gate 301G of the upper arm switching element T1 are electrically

connected to the upper arm switching element driving signal output terminal UPo of the high proof pressure IC 100 (omitted in drawing 11) through the bonding wire W2.
[0145] By anode 302A, the front face is formed by the upper arm diode chip 302 so that a rear face may serve as cathode 302C. Cathode 302C of diode D1 is directly in contact with the bonding pad P, and anode 302A is electrically connected to the bonding pad U through wire W3. Although not limited especially, in drawing 11 , wire W3 serves as a wire bundle which consists of three wires.
[0146] Gate 303G (field surrounded squarely) are prepared in a part of the front face, and the bottom arm switching element chip 303 is formed so that chip front faces other than the field which is gate 303G may serve as collector 303C. The rear face of the bottom arm switching element chip 303 is emitter 303E. Collector 303C of the bottom arm switching element T2 is directly in contact with the bonding pad U.
[0147] Emitter 303E of the bottom arm switching element T2 is electrically connected to the bonding pad N through the wire W4. Although not limited especially, in drawing 11 , the wire W4 serves as a wire bundle which consists of three wires. Gate 303G of the bottom arm switching element T2 are electrically connected to the bottom arm switching element driving signal output terminal UNo of the high proof pressure IC 100 (omitted in drawing 11) through the bonding wire W5.
[0148] By anode 304A, the front face is formed by the bottom arm diode chip 304 so that a rear face may serve as cathode 304C. Cathode 304C of diode D2 is directly in contact with the bonding pad U, and anode 304A is electrically connected to the bonding pad N through the wire W6. Although not limited especially, in drawing 11 , the wire W6 serves as a wire bundle which consists of three wires.
[0149] Moreover, anode 304A of the bottom arm diode chip 304 is electrically connected to the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 100 (illustration abbreviation) through the bonding wire W7. Near the bottom arm diode chip 304 of a bonding pad U, the bonding wire W7 connected to the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 (illustration abbreviation) is connected electrically.
[0150] The circuit diagram of the inverter circuit of a configuration of being shown in drawing 11 is shown in drawing 12 . The wiring section which attached hatching in drawing 12 is the bonding pad of Above P, U, and N, and the wiring section shown as the continuous line is a bonding wire. According to the configuration shown in drawing 11 , it turns out that the bonding wire W8 which the bonding wire W7 connected to the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 100 (illustration abbreviation) from anode 304A of diode D2 was pulled out, and was connected to the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 (illustration abbreviation) near cathode 304C of diode D2 is pulled out so that clearly from this drawing.
[0151] In addition, in drawing 11 and drawing 12 , the wiring section which attached signs X1 and X0, and was shown with the broken line is a bonding wire with which connection with the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides in the conventional inverter circuit is presented, respectively.
[0152] Since according to the gestalt 4 of this operation a bonding wire W7 is connected to anode 304A of diode D2 and the bonding wire W8 is connected near cathode 304C of diode D2, as explained above, In not forming a current detector, the amount of [by the inductances La and Lb (refer to drawing 12) produced with the conventional circuit pattern] electrical-potential-difference generating loses. The negative electrical potential difference which may be impressed between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0 is ON state voltage VF (usually) of diode D2 mostly. It is prevented that a less [than rated proof-pressure minimum value-5V] negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 since it becomes. even if high -- about 3V -- it is only -- Proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0153] moreover, when the current detector 106 is formed according to the gestalt 4 of this operation Although the negative electrical potential difference by various factors which were explained with the above-mentioned conventional technique besides ON-state-voltage VF of diode D2 occurs and is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0 Since it decreases about a part for electrical-potential-difference generating by the inductances La and Lb (refer to drawing 12) produced with the conventional circuit pattern If the negative electrical potential difference generated by the current detector 106 among the up-and-down arm switching element driving signal criteria output terminals VS [VS1 and] 0 is low, proof-pressure destruction of the high proof pressure IC 100 can be prevented.
[0154] (Gestalt 5 of operation) Drawing 13 is the mimetic diagram showing the example of chip arrangement of the inverter circuit when not forming the current detector of the three-phase-circuit inverter equipment concerning this invention.
[0155] This inverter circuit Each chip of the upper arm switching element T1, T3, and T5 Each chip of diodes D1, D3, and D5 by which antiparallel connection was carried out to 401,402,403 and the upper arm switching element T1, T3, and T5, respectively (An upper arm switching element chip is called hereafter) Each chip of 407,408,409, the bottom arm switching element T2, T four, and T6 (An upper arm diode chip is called hereafter) Each chip of diodes D2, D4, and D6 by which antiparallel connection was carried out to 404,405,406 and the bottom arm switching element T2, T four, and T6, respectively (A bottom arm switching element chip is called hereafter) The bonding pad used as the power supply terminal P which impresses forward supply voltage to 410,411,412 and an inverter circuit (A bottom arm diode chip is called hereafter) (In the gestalt 5 of this operation, it considers as a bonding pad P hereafter) The bonding pad used as the power supply terminal N which impresses negative supply voltage to an inverter circuit Each bonding pad used as the output terminals U, V, and W of (it considers as a bonding pad N similarly hereafter), and an inverter circuit The bonding pad of dedication to which the bonding wire W10 connected to the bottom arm switching element driving signal criteria output terminal VS 0 (which it lets hereafter be bonding pads U, V, and W similarly, respectively) is connected electrically (The bonding pad for VS0 is called hereafter) It has composition equipped with 420.
[0156] Gates 401G, 402G, and 403G (field surrounded squarely) are established in a part of the front face, respectively, and the upper arm switching element chip 401,402,403 is formed so that chip front faces other than the field which are each gates 401G, 402G, and 403G may serve as Collectors 401C, 402C, and 403C, respectively. The rear face of each up arm switching element chip 401,402,403 serves as Emitters 401E, 402E, and 403E, respectively. Each up arm switching element T1, T3, and the collectors 401C, 402C, and 403C of T5 are directly in contact with the bonding pad P. Each up arm switching element T1, T3, and the emitters 401E, 402E, and 403E of T5 are electrically connected to the bonding pad U through wires W11, W12, and W13, respectively.
[0157] Although not limited especially, in drawing 13 , wires W11, W12, and W13 serve as a wire bundle which all consists of three wires. Each up arm switching element T1, T3, and the gates 401G, 402G, and 403G of T5 are electrically connected to the upper arm switching element driving signal output terminals UPo, VPo, and WPo of the high proof pressure IC 200 (illustration abbreviation) through the bonding wire (illustration abbreviation), respectively.
[0158] With Anodes 407A, 408A, and 409A, each front face is formed by the upper arm diode chip 407,408,409 so that each rear face may serve as Cathodes 407C, 408C, and 409C. The cathodes 407C, 408C, and 409C of each diodes D1, D3, and D5 are directly in contact with the bonding pad P, and Anodes 407A, 408A, and 409A are electrically connected to the bonding pad U through wires W14, W15, and W16. Although not limited especially, in drawing 13 , each of wires W14, and 15 and 16 is the wire bundle which consists of three wires.
[0159] Gates 404G, 405G, and 406G (field surrounded squarely) are established in a part of each front face, and the bottom arm switching element chip 404,405,406 is formed so that chip front faces other than the field which are each gates 404G, 405G, and 406G may serve as Collectors 404C, 405C, and 406C, respectively. The rear face of each Shimo arm switching element chip 404,405,406 serves as

Emitters 404E, 405E, and 406E, respectively.
[0160] Each Shimo arm switching element T2, T four, and the collectors 404C, 405C, and 406C of T6 are directly in contact with the bonding pad U. Each Shimo arm switching element T2, T four, and the emitters 404E, 405E, and 406E of T6 are electrically connected to the bonding pad N through wires W17, W18, and W19, respectively. Although not limited especially, in drawing 13 , wires W17, W18, and W19 serve as a wire bundle which all consists of three wires. Each Shimo arm switching element T2, T four, and the gates 404G, 405G, and 406G of T6 are electrically connected to the bottom arm switching element driving signal output terminals UNo, VNo, and WNo of the high proof pressure IC 200 (illustration abbreviation) through the bonding wire (illustration abbreviation), respectively.
[0161] With Anodes 410A, 411A, and 412A, each front face is formed by the bottom arm diode chip 410,411,412 so that each rear face may serve as Cathodes 410C, 411C, and 412C. The cathodes 410C, 411C, and 412C of each diodes D2, D4, and D6 are directly in contact with the bonding pad U, and Anodes 410A, 411A, and 412A are electrically connected to the bonding pad N through wires W20, W21, and W22. Although not limited especially, in drawing 13 , each of wires W20, and 21 and 22 is the wire bundle which consists of three wires.
[0162] Moreover, the anodes 410A, 411A, and 412A of each Shimo arm diode chip 410,411,412 are electrically connected to the bonding pad 420 for VS0 through a bonding wire W23, and 24 and 25, respectively.
[0163] Furthermore, each bonding pads U, V, and W are electrically connected to the wiring section 421,422,423 by which pattern shaping was carried out through bonding wires W26, W27, and W28 near the bottom arm diode chip 410,411,412, respectively. Each wiring section 421,422,423 is electrically connected to the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 (illustration abbreviation) through a bonding wire W29, and 30 and 31, respectively.
[0164] As explained above, according to the gestalt 5 of this operation While the current which becomes main for the wiring path which results in each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 from the cathodes 410C, 411C, and 412C of each diodes D2, D4, and D6 of a bottom arm flows Since the current which becomes main also for the wiring path which results in the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 200 from the anodes 410A, 411A, and 412A of each diodes D2, D4, and D6 flows The electrical potential difference V impressed among the arm switching element driving signal criteria output terminals VS1, VS2, VS3, and VS0 of these upper and lower sides (VS1-VS0) V (VS2-VS0) and V (VS3-VS0) become only ON state voltage VF of each diodes D2, D4, and D6, and can prevent proof-pressure destruction of the high proof pressure IC 200.
[0165] moreover, when the current detector 214 is formed according to the gestalt 5 of this operation Between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 Although the negative electrical potential difference by various factors which were explained with the above-mentioned conventional technique besides ON-state-voltage VF of diodes D2, D4, and D6 occurs and is impressed Since it decreases about a part for electrical-potential-difference generating by the inductance produced with the conventional circuit pattern If the negative electrical potential difference generated by the current detector 214 among the up-and-down arm switching element driving signal criteria output terminals VS1, VS2, VS3, and VS0 is low, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0166] (Gestalt 6 of operation) Next, the gestalt 6 of operation concerning this invention is explained. The description of the gestalt 6 of this operation is using what has larger current capacity than the switching element and diode of others [diode] by which antiparallel connection's was carried out to the bottom arm switching element among two or more switching elements and diodes which are used for the inverter circuit. That is, it is because ON state voltage VF of this diode will become low and the negative electrical potential difference impressed between the arm switching element driving signal criteria output terminals of the upper and lower sides of the high proof pressure IC will become smaller,

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is applied to proof-pressure destructive prevention of the high proof-pressure IC which drives the bridge circuit of inverter equipment to an inverter equipment pan, and relates to an effective technique.
[0002]
[Description of the Prior Art] Conventionally, what was indicated by JP,4-54461,A as the current detection approach is known about the inverter circuit of a three phase circuit. The outline of the configuration of the three-phase-circuit inverter circuit indicated by the JP,4-54461,A is shown in drawing 15 . This three-phase-circuit inverter circuit has six switching elements T1 and T2 which consist of npn transistors, T3, T four, T5 and T6, each [these] switching elements T1 and T2 and T3, T four, and the electrical-potential-difference form inverter 1 that consists of six diodes D1, D2, D3, D4, D5, and D6 connected to juxtaposition T5 and T6, respectively.
[0003] Moreover, driving gears, such as a load of the motor 2 grade driven by this inverter circuit and six switching elements T1 and T2, T3, T four, and the high proof pressure IC (illustration abbreviation) that drives T5 and T6, are connected to this three-phase-circuit inverter circuit. Furthermore, the current detector 3 is formed in this three-phase-circuit inverter circuit. And the output voltage of the current detector 3 is changed into a digital signal by the A/D (analog/digital) transducer 4, and a processor (CPU) 5 is supplied. The interruption pulse generator 6 which generates the seizing signal of interrupt processing of this CPU5 is connected to CPU5. CPU5 is programmed to perform processing of predetermined interruption routine, if the current value detected by the current detector 3 turns into a predetermined value.
[0004] A switching element T1, T3, and T5 are the switching elements by the side of an upper arm (an upper arm switching element is called hereafter, respectively), respectively. A switching element T2, T four, and T6 are the switching elements by the side of a bottom arm (a bottom arm switching element is called hereafter, respectively), respectively. The upper arm switching element T1, the bottom arm switching element T2, upper arm switching element T3, bottom arm switching element T four and the upper arm switching element T5, and the bottom arm switching element T6 serve as a pair, respectively, and constitute the inverter of a three phase circuit.
[0005] Forward supply voltage is impressed to each up arm switching element T1, T3, and the collector of T5. Each up arm switching element T1, T3, and the emitter of T5 are connected to the bottom arm switching element T2, T four, and the collector of T6, respectively. Common connection of each Shimo arm switching element T2, T four, and the emitter of T6 is made, and they are connected to the negative supply voltage line through the current detector 3. Each up arm switching element T1, T3, T5 and each Shimo arm switching element T2, T four, and the gate of T6 are connected to the driving signal output terminal (illustration abbreviation) of driving gears, such as the high proof pressure IC, and each switching elements T1 and T2, T3, T four, and T5 and T6 are driven with the driving signal supplied from the driving gear (illustration abbreviation).

[0006] Moreover, the cathode of diodes D1, D3, and D5 is connected to each up arm switching element T1, T3, and the collector of T5, respectively, and the anode of diodes D1, D3, and D5 is connected to each up arm switching element T1, T3, and the emitter of T5, respectively. Moreover, the cathode of diodes D2, D4, and D6 is connected to each Shimo arm switching element T2, T four, and the collector of T6, respectively. The anode of diodes D2, D4, and D6 is connected to the direct negative supply voltage line, without minding the current detector 3. Namely, antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 is carried out to switching elements T1 and T2, T3, T four, and T5 and T6, respectively.
[0007] The three-phase-circuit inverter circuit shown in drawing 15 detects the current which comes to compound only each Shimo arm switching element T2, T four, and the current that flows T6 with the current detector 3 by being constituted as mentioned above. The inverter circuit of a configuration of being shown in this drawing 15 is often used conventionally.
[0008] The three-phase-circuit inverter circuit shown in drawing 16 forms the current detector 7 in the wiring path of a drive current of flowing for the load of motor 2 grade from this inverter circuit, instead of forming the current detector 3 between the bottom arm switching element T2, T four, and each emitter of T6 and a negative supply voltage line, as shown in drawing 15. The configuration of the electrical-potential-difference form inverter 1 with which it comes to carry out antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 to six switching elements T1 and T2, T3, T four, and T5 and T6, respectively is the same as the configuration shown in drawing 15 . The inverter circuit of a configuration of being shown in this drawing 16 is also often used conventionally. In addition, although the illustration abbreviation was carried out, it cannot be overemphasized that A/D converter 4, CPU5, and the interruption pulse generator 6 are connected so that interrupt processing can be performed to the current detector 7 according to a detection current value.
[0009] The three-phase-circuit inverter circuit shown in drawing 17 forms the current detector 8 in the bus-bar which comes to make common connection of the bottom arm switching element T2, T four, and each emitter of T6, each anode of the diodes D2, D4, and D6 and each instead of forming the current detector 3 between the bottom arm switching element T2, T four, and each emitter of T6 and a negative supply voltage line, as shown in drawing 15 .
[0010] The configuration of the electrical-potential-difference form inverter 1 with which it comes to carry out antiparallel connection of the diodes D1, D2, D3, D4, D5, and D6 to six switching elements T1 and T2, T3, T four, and T5 and T6, respectively is the same as the configuration shown in drawing 15 . The inverter circuit of a configuration of being shown in this drawing 17 is also often used conventionally. In addition, although the illustration abbreviation was carried out, it cannot be overemphasized that A/D converter 4, CPU5, and the interruption pulse generator 6 are connected so that interrupt processing can be performed to the current detector 7 according to a detection current value.
[0011] The common single phase inverter equipment it was made to drive the arm switching element of the upper and lower sides of an inverter circuit with the high proof pressure IC is shown in drawing 18 . The single phase inverter circuit of this example is the thing of a configuration of being equivalent to the inverter part of the plane 1 of the three-phase-circuit inverter circuits shown in drawing 17 . That is, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.
[0012] And the current detector 106 is formed on the bus-bar with which common connection of the anode of the diode D2 by which antiparallel connection was carried out to the emitter of the bottom arm switching element T2 and it is made, and it results in the terminal by the side of negative (-) of DC power supply 108. Common connection of the cathode of the diode D1 by which antiparallel connection was carried out to the collector of the upper arm switching element T1 and it is made at the terminal by the side of forward (+) of DC power supply 108. A driving signal is inputted into each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2 from the high proof pressure IC 100, respectively.

[0013] Moreover, three external connection terminals P, U, and N are formed in the inverter circuit of the above-mentioned configuration. The external connection terminal P is the power supply terminal which impresses forward supply voltage to an inverter circuit, i.e., the terminal with which common connection of the collector of the upper arm switching element T1 and the cathode of diode D1 was made. The emitter of the power supply terminal T2 with which the external connection terminal N impresses negative supply voltage to an inverter circuit, i.e., a bottom arm switching element, and the anode of diode D2 are the terminals by which the other end of the current detector 106 by which common connection was made was connected to the end.
[0014] That is, the external connection terminal P is connected as a forward side in DC power supply 108 between the external connection terminal P and the external connection terminal U. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1. And between the external connection terminal U and the external connection terminal N, the reactor (inductance value: LL) 107 is connected as a load.
[0015] The parasitism reactor of L1 exists [an inductance value] in the wiring section between the connection node E1 and the collector of the bottom arm switching element T2. The parasitism reactor of L2 exists [an inductance value] in the cathode side wiring section of diode D2. The parasitism reactor of L3 and L4 exists [an inductance value] in a serial at the anode side wiring section of diode D2. The parasitism reactor of L5 exists [an inductance value] in wiring between the connection node E0 and the connection node N1 prepared in the opposite side (namely, between the current detector 106 and the external connection terminals N) of E0 on both sides of the current detector 106.
[0016] In addition, power-source body 108a and capacitor 108b which generate electromotive force are connected to juxtaposition, and DC power supply 108 are constituted.
[0017] The high proof pressure IC 100 The driving signal input terminals UPi and UNi of this IC100 are minded. The signal inputted from the outside The output signal of the input buffer a1 held temporarily, the level shifter a2 which generates the signal of the floating potential which received the output signal of the input buffer a1, and floated from the potential of the signal, and a level shifter a2 is received. The upper arm switching element T1 The detecting signal outputted from the bottom arm side driver circuit a4 which receives the output signal of the upper arm side driver circuit a3 to drive and an input buffer a1, and drives the bottom arm switching element T2, the overcurrent detector a5 which performs detection of an overcurrent, and the overcurrent detector a5 It has the error signal generator a6 which receives and generates an error signal.
[0018] The upper arm side driver circuit a3 outputs a driving signal to the upper arm switching element T1 through the upper arm switching element driving signal output terminal UPo prepared in the high proof pressure IC 100. Moreover, a forward and negative floating electrical potential difference is impressed to the high proof pressure IC 100 from the outside in the upper arm side driver circuit a3 through the floating power-source forward side input terminal VB 1 prepared, respectively and the floating power-source negative side input terminal VS 1. The floating power-source negative side input terminal VS 1 serves as the upper arm switching element driving signal criteria output terminal.
[0019] The bottom arm side driver circuit a4 outputs a driving signal to the bottom arm switching element T2 through the bottom arm switching element driving signal output terminal UNo prepared in the high proof pressure IC 100. Moreover, forward supply voltage is impressed to the bottom arm side driver circuit a4 from the outside through the forward side power supply terminal VCC prepared in the high proof pressure IC 100. The bottom arm side driver circuit a4 is connected to the bottom arm switching element driving signal criteria output terminal VS 0 prepared in the high proof pressure IC 100.
[0020] The overcurrent detector a5 is connected to the current detection terminal OC prepared in the high proof pressure IC 100.
[0021] The error signal generator a6 outputs an error signal to a control unit, an alarm information means, etc. which the exterior does not illustrate through the error output terminal Fo prepared in the high proof pressure IC 100.
[0022] The forward side power supply terminal VCC and the negative side power supply terminal VSS

which were prepared in the high proof pressure IC 100, respectively are connected to the positive electrode and negative electrode of an external power 101, respectively. And the negative side power supply terminal VSS is grounded.

[0023] External [of the diode 102, the capacitor 103, and reference diode 109 other than the above-mentioned external power 101] is carried out to the high proof pressure IC 100. Namely, the anode is connected to the forward side power supply terminal VCC, and, as for diode 102, the cathode is connected to the floating power-source forward side input terminal VB 1. The capacitor 103 is connected between the floating power-source forward side input terminal VB 1 and the floating power-source negative side input terminal VS 1. Reference diode 109 is formed in the overvoltage protections of the bottom arm switching element driving signal criteria output terminal VS 0, and is connected between the bottom arm switching element driving signal criteria output terminal VS 0 and the negative side power supply terminal VSS.

[0024] The high proof pressure IC 100 is connected to the inverter circuit which consists of the arm switching elements T1 and T2 and DC power supply 108 of a vertical pair as follows. That is, the floating power-source negative side input terminal (upper arm switching element driving signal criteria output terminal) VS 1 of the high proof pressure IC 100 is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1. The upper arm switching element driving signal output terminal UPo is connected to the gate G1 of the upper arm switching element T1 through gate resistance 104.

[0025] Moreover, the bottom arm switching element driving signal criteria output terminal VS 0 is connected to the connection node E0 by the side of the emitter of the bottom arm switching element T2. The bottom arm switching element driving signal output terminal UNo is connected to the gate G2 of the bottom arm switching element T2 through gate resistance 105. The current detection terminal OC is connected to said connection node E0. Moreover, the negative side power supply terminal VSS is connected to said connection node N1 of an inverter circuit. Since the current detector 106 is between these connection node E0 and the connection node N1 as mentioned above, the detection electrical potential difference of the current detector 106 will be impressed to the current detection terminal OC.

[0026] L6 and the parasitism reactor of L7 exist [the inductance value] in wiring between the bottom arm switching element driving signal criteria output terminal VS 0 and the connection node E0, and wiring between the negative side power supply terminal VSS and the connection node N1, respectively.

[0027] The maximum of pressure-proofing here of the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) +600] bolt extent, although there are some differences by the application, and the thing of the minimum value of any applications is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent. That is, between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, it means that the electrical potential difference not more than -5V cannot be applied.

[0028] Since this is guaranteed only about -0.5V to the potential below the supply voltage of the IC also by IC which generally consists of an IC which consists of CMOSFET(s) (insulated gate field effect transistor of a complementary type), or TTL (transistor transistor logic) of BAIPORA, it is considered to be because it to become weak theoretically to the potential below supply voltage.

[0029] The timing of the inverter equipment shown in drawing 18 of operation is shown in drawing 19 . In drawing 19 , S (UPo) and S (UNo) are the signals outputted from the upper arm switching element driving signal output terminal UPo of the high proof pressure IC 100, and the bottom arm switching element driving signal output terminal UNo, respectively, and are the driving signal of the upper arm switching element T1 and the bottom arm switching element T2, respectively. Moreover, the current on which I1 flows the upper arm switching element T1, the current to which I2 flows to diode D2, and I3 are currents which flow a reactor 107.

[0030] Each driving signal S (UPo) and S (UNo) of the up-and-down arm switching elements T1 and T2 of the up-and-down arm switching elements T1 and T2 is all an OFF state relatively in the condition of

low voltage (low) level (it considers as L level hereafter). Therefore, the driving signals S (UPo) and S (UNo) of L level are switching element off signals.

[0031] When driving signals S (UPo) and S (UNo) are all switching element off signals (namely, L level) If a driving signal S (UPo) starts and it changes to the signal (namely, switching element ON signal) of high potential (yes) level (it considers as H level hereafter) relatively While a driving signal S (UPo) is H level (period of A in drawing 19), a current flows through the external connection terminal P, the upper arm switching element T1, a reactor 107, and the external connection terminal N in the path of negative-electrode HE **** of DC power supply 108 from the positive electrode of DC power supply 108.

[0032] Here, in the inverter equipment shown in drawing 18 , if time amount width of face (period of A) Ton in case 3mH(s) and a driving signal S (UPo) are H level about the inductance value LL of 300V and a reactor 107 in the output voltage VDC of DC power supply 108 is set to 1ms, the peak current Ip of a reactor 107 will be set to 100A (ampere) from the following formula.

Ip=VDC-Ton/LL= {300and1- (E-3)} /{3- (E-3)}
=100[A]

In addition, that it is with "(E-n)" means - (minus) n-th power of 10 among this specification. However, n is the natural number.

[0033] Then, if a driving signal S (UPo) falls and it is set to L level, the upper arm switching element T1 will change to an OFF state. By it, the current I1 which flows the upper arm switching element T1 begins to decrease, and only predetermined time amount (period of B in drawing 19) is in it, and it becomes zero. On the other hand, the current I2 which flows diode D2 begins to increase synchronizing with the fall edge of a driving signal S (UPo), and reaches said peak current Ip after period progress of B. By the period of this B, since the variation (di/dt) per unit time amount of a current is large, several V induced voltage occurs also in few wiring inductances. Moreover, diode D2 will generate the ON state voltage of about 2v, if a current flows.

[0034] In the inverter equipment shown in drawing 18 here the synthetic inductance value of the wiring inductances L1, L2, L3, and L4 20nH(s), If switching speed Toff of 2V and the upper arm switching element T1 is set to 400ns for ON state voltage VF of diode D2 and value 100A of the above-mentioned peak current Ip is used The electrical potential difference V (E1-E0) built between the connection node E1 by the side of the emitter of the upper arm switching element T1 and the connection node E0 by the side of the emitter of the bottom arm switching element T2 is set to -7V from the following formula.

400and [V(E1-E0) =- (L1+L2+L3+L4) and Ip/Toff-VF=-{20-(E-9) -100}// {and / and (E-9) /}] -2=-7 [V]

[0035] Thus, even if a wiring inductance is small, if a high current flows like the period of B of drawing 19 , the electrical potential difference exceeding the pressure-proofing by the side of minus of the high proof pressure IC 100, i.e., [(potential of VS0) -5] bolt, (it is less than the minimum value) will occur.

[0036] Moreover, if the wiring inductance L5 is set to 20nH(s) and 400ns of values of the switching speed Toff of value 100A of the above-mentioned peak current Ip and the upper arm switching element T1 is used The electrical potential difference V (E0-N1) by which induction is carried out at the period of B of drawing 19 on both sides of the connection node E0 and the current detector 106 by the side of the emitter of the bottom arm switching element T2 between the connection nodes N1 of the opposite side of this connection node E0 is set to -5V by the following formula.

V(E0-N1) =-L5 and Ip/Toff=-{20-(E-9) -100}/{400- (E-9)}
=-5[V]

[0037] A current flows for the path from the connection node N1 to [with this electrical potential difference V (E0-N1) by which induction was carried out] the connection node E0 through the parasitism reactor of the wiring inductance value L7, reference diode 109, and the parasitism reactor of wiring inductance value L6. Supposing wiring inductance value L6 and L7 are equal here, induced voltage V (E0-N1) will take every [2 / 1/] between the negative side power supply terminal VSS and the connection node N1 and between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0. Therefore, the electrical potential difference V (VSS-N1) which

acts at the period of B of drawing 19 between the negative side power supply terminal VSS and the connection node N1 is set to -2.5V by the following formula.
V(VSS-N1)=V(E0-N1)/2=-2.5[V]
[0038] Moreover, the electrical potential difference V (E0-VS0) which acts between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0 is set to -2.5V by the following formula at the period of B of drawing 19 .
V(E0-VS0)=V(E0-N1)/2=-2.5[V]
[0039] In addition, in the period of B of drawing 19 , since especially an electrical potential difference is not built between the upper arm switching element driving signal criteria output terminal VS 1 and the connection node E1, the electrical potential difference V between them (VS1-E1) is 0V.
[0040] The electrical potential difference V (VS1-VS0) which acts among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides at the period of B of drawing 19 is set to -9.5V from the above-mentioned consideration from the following formula.
V(VS1-VS0)=V(VS1-E1)+V(E1-E0)+V(E0-VS0
=0-7-2.5=-9.5[V]
[0041] Thus, even if a wiring inductance is small, if a high current flows like the period of B of drawing 19 , the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing (-5V) among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides of the high proof pressure IC 100 will be carried out, and the high proof pressure IC 100 will cause proof-pressure destruction.
[0042] Other examples of the common single phase inverter equipment it was made to drive the arm switching element of the upper and lower sides of an inverter circuit with the high proof pressure IC are shown in drawing 20 . The single phase inverter circuit of this example is the thing of a configuration of being equivalent to the inverter part of the plane 1 of the three-phase-circuit inverter circuits shown in drawing 15 . That is, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.
[0043] And the emitter of the bottom arm switching element T2 is connected to the end of the current detector 106. The other end of the current detector 106 is connected to the negative electrode of DC power supply 108 through the external connection terminal N. The anode of diode D2 is connected to the negative side power supply terminal VSS of the high proof pressure IC 100. Common connection of the collector of the upper arm switching element T1 and the cathode of diode D1 is made, and they are connected to the external connection terminal P at the terminal by the side of forward (+) of DC power supply 108. A driving signal is inputted into each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2 from the high proof pressure IC 100, respectively.
[0044] In addition, about the configuration of others of an inverter circuit, the configuration of the high proof pressure IC 100, and connection between an inverter circuit and the high proof pressure IC 100, since it is the same as the thing of a configuration of being shown in drawing 18 , the explanation which attaches the same sign and overlaps is omitted.
[0045] the electrical potential difference V (E1-E0) built [like the example of a configuration of drawing 18 mentioned above also in the example of the configuration of this drawing 20] between the connection node E1 by the side of the emitter of the upper arm switching element T1, and the connection node E0 by the side of the emitter of the bottom arm switching element T2 with the electrical potential difference in which induction was carried out by the wiring inductance of ON state voltage VF of diode D2, or the chip of diode D2 and the bottom arm switching element T2 -- about -- it is set to -7V.
[0046] In addition, 400ns and the peak current Ip are set [the synthetic inductance value of the wiring inductances L1, L2, L3, and L4 / ON state voltage VF of 20nH(s) and diode D2] to 100A for the switching speed Toff of 2V and the upper arm switching element T1 like the consideration about the configuration of drawing 18 . However, in the example of this drawing 20 , since the current which flows diode D2 does not pass along the current detector 106, between the connection node E0 and the

bottom arm switching element driving signal criteria output terminal VS 0, an electrical potential difference does not generate it.

[0047] Therefore, the electrical potential difference of V (E1-E0) is built as it is between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0. That is, between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, the seal of approval of the electrical potential difference (-7V) which is less than (-5V) will be carried out in the minimum range of rated pressure-proofing, and the high proof pressure IC 100 will cause proof-pressure destruction.

[0048] Moreover, at the moment of the current which was flowing to the bottom arm switching element T2 being intercepted, an electrical potential difference occurs with the parasitism reactor of the wiring inductance value L5 which is parasitic between the connection node E0 and the current detector 106, and the partial pressure of the generated electrical potential difference is carried out to wiring inductance value L6 and each parasitism reactor of L7.

[0049] Therefore, an electrical potential difference V (E0-VS0) occurs between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0. Like the consideration about the configuration of drawing 18 , if the wiring inductance L5 is set to 20nH(s) and switching speed Toff of 100A and the upper arm switching element T1 is set to 400ns for the peak current Ip, V (E0-VS0) will turn into -2.5V.

[0050] Among the connection nodes E1 and E0, an electrical potential difference V (E1-E0) occurs with the parasitism reactor of the wiring inductance value L1, the reactor, and ON state voltage Vce of a switching element T2 of the synthetic inductance value L8 which is parasitic on the circuit pattern of the bottom arm switching element T2. In the synthetic inductance value of L1 and L8, if 20nH(s) and said Vce are set to 2V and switching speed Toff of 100A and the upper arm switching element T1 is set to 400ns for the peak current Ip, the value of an electrical potential difference V (E1-E0) will be set to -3V from the following formula.

V(E1-E0)=-(L1+L8)
- Ip/Toff+Vce =-{20 -(E-9)- 100}
/{400- (E-9)} +2 = -3 [V]

[0051] In addition, since especially an electrical potential difference is not built between the upper arm switching element driving signal criteria output terminal VS 1 and the connection node E1, the electrical potential difference V between them (VS1-E1) is 0V.

[0052] The electrical potential difference V (VS1-VS0) which acts among the up-and-down arm switching element driving signal criteria output terminals VS1 and VS0 is set to -5.5V from the above-mentioned consideration from the following formula.

V(VS1-VS0)=V(VS1-E1
+V(E1-E0)
+V(E0-VS0)
=0-3-2.5=-5.5[V]

[0053] Thus, also in the equipment of a configuration of being shown in drawing 20 , if a high current flows, the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing (-5V) among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides of the high proof pressure IC 100 will be carried out, and the high proof pressure IC 100 will cause proof-pressure destruction.

[0054] Although the value of an electrical potential difference V (VS1-VS0) changes with methods of arrangement [consideration / about the equipment of a configuration of being shown in above-mentioned drawing 18 and drawing 20 , respectively / above-mentioned] of the current detector 106 Under the effect by few inductances of wiring of a chip, or few inductances of wiring of the current detector 106 It turns out that the minus electrical potential difference which is less than the minimum value of rated pressure-proofing among the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides to the case of a high current drive may occur.

[0055] About the consideration mentioned above, the minus electrical potential difference which is the same when not forming a current detector (i.e., also when not performing current detection), as shown in drawing 21 , and is less than the minimum value of rated pressure-proofing with few inductances of wiring of a chip among the up-and-down arm switching element driving signal criteria output terminals VS1 and VS0 in a high current drive may occur. Therefore, the high proof pressure IC 100 will cause proof-pressure destruction. In addition, reference diode 109 is not formed with the inverter equipment of a configuration of being shown in drawing 21 .

[0056] The common three-phase-circuit inverter equipment it was made to drive the arm switching element of three pairs of upper and lower sides of an inverter circuit with the high proof pressure IC is shown in drawing 22 . The three-phase-circuit inverter circuit of this example is the thing of a configuration of being equivalent to the three-phase-circuit inverter circuit shown in drawing 17 . That is, in eye the 1st phase, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.

[0057] In eye the 2nd phase, antiparallel connection of the up-and-down diodes D3 and D4 is carried out to switching element T3 of the pair to which it comes to connect the emitter of upper arm switching element T3, and the collector of bottom arm switching element T four, and T four, respectively. In eye the 3rd phase, antiparallel connection of the up-and-down diodes D5 and D6 is carried out to the switching elements T5 and T6 of a pair with which it comes to connect the emitter of the upper arm switching element T5, and the collector of the bottom arm switching element T6, respectively.

[0058] And common connection of the anode of the diodes D2, D4, and D6 by which antiparallel connection was carried out to each Shimo arm switching element T2, T four, the emitter of T6, and them is made, and common connection is made at the end of the current detector 214. The other end of the current detector 214 is connected to the external connection terminal N. Common connection of the cathode of the diodes D1, D3, and D5 by which antiparallel connection was carried out to each up arm switching element T1, T3, the collector of T5, and them is made at the external connection terminal P. A driving signal is inputted into each up arm switching element T1, T3, the gate G1 of T5, G3, G5 and each Shimo arm switching element T2, T four, and the gates G2, G4, and G6 of T6 from the high proof pressure IC 200, respectively.

[0059] Moreover, three external connection terminals U, V, and W are formed in the inverter circuit of the above-mentioned configuration in addition to the above-mentioned external connection terminals P and N. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1 of eye the 1st phase. The external connection terminal U is connected to the connection node E1 by the side of the emitter of the upper arm switching element T1 of eye the 1st phase. The external connection terminal V is connected to the connection node E2 by the side of the emitter of upper arm switching element T3 of eye the 2nd phase. The external connection terminal W is connected to the connection node E3 by the side of the emitter of the upper arm switching element T5 of eye the 3rd phase.

[0060] Although not illustrated especially, a parasitism reactor exists in each Shimo arm switching element T2, T four, the wiring section of T6, and the wiring section of each diodes D2, D4, and D6, respectively. Moreover, a parasitism reactor exists also in wiring between the connection node E0 by the side of each Shimo arm switching element T2, T four, and the emitter of T6, and the connection node N1 prepared in the opposite side (namely, between the current detector 214 and the external connection terminals N) of E0 on both sides of the current detector 214.

[0061] The high proof pressure IC 200 The driving signal input terminals UPi, UNi, VPi, VNi, WPi, and WNi of this IC200 are minded. The signal inputted from the outside Each output signal of three level shifters b2, b3, and b4 and level shifters b2, b3, and b4 which generates the signal of the input buffer b1 held temporarily and the floating potential which received the output signal of the input buffer b1, and floated from the potential of the signal It receives and three signals outputted from the upper arm switching element T1, T3, the three upper arm side driver circuits b5, b6, and b7 that drive T5, and an input buffer b1, respectively are received., respectively the bottom arm switching element T2, T four,

and T6 It has the bottom arm side driver circuits b8, b9, and b10 to drive, the overcurrent detector b11 which performs detection of an overcurrent, and the error signal generator b12 which receives the detecting signal outputted from the overcurrent detector b11, and generates an error signal.
[0062] Each up arm side driver circuits b5, b6, and b7 output a driving signal to each up arm switching element T1, T3, and T5 through the upper arm switching element driving signal output terminals UPo, VPo, and WPo prepared in the high proof pressure IC 200, respectively. Moreover, a forward and negative floating electrical potential difference is impressed to the high proof pressure IC 200 from the outside in each up arm side driver circuits b5, b6, and b7 through the floating power-source forward side input terminals VB1, VB2, and VB3 and the floating power-source negative side input terminals VS1, VS2, and VS3 which were prepared, respectively. Each floating power-source negative side input terminals VS1, VS2, and VS3 serve as each up arm switching element T1, T3, and the upper arm switching element driving signal criteria output terminal of T5, respectively.
[0063] Each Shimo arm side driver circuits b8, b9, and b10 output a driving signal to each Shimo arm switching element T2, T four, and T6 through the bottom arm switching element driving signal output terminals UNo, VNo, and WNo prepared in the high proof pressure IC 200, respectively. Moreover, forward supply voltage is impressed to each Shimo arm side driver circuits b8, b9, and b10 from the outside through the forward side power supply terminal VCC prepared in the high proof pressure IC 200. Common connection of each Shimo arm side driver circuits b8, b9, and b10 is made at the bottom arm switching element driving signal criteria output terminal VS 0 prepared in the high proof pressure IC 200.
[0064] The overcurrent detector b11 is connected to the current detection terminal OC prepared in the high proof pressure IC 200.
[0065] The error signal generator b12 outputs an error signal to a control unit, an alarm information means, etc. which the exterior does not illustrate through the error output terminal Fo prepared in the high proof pressure IC 200.
[0066] The forward side power supply terminal VCC and the negative side power supply terminal VSS which were prepared in the high proof pressure IC 200, respectively are connected to the positive electrode and negative electrode of an external power 201, respectively. And the negative side power supply terminal VSS is grounded.
[0067] External [of the capacitor 205,206,207 of three diodes / 202,203,204 of 3 / and reference diode 215 other than the above-mentioned external power 201] is carried out to the high proof pressure IC 200. Namely, common connection of each anode is made at the forward side power supply terminal VCC, and, as for diode 202,203,204, each cathode is connected to the floating power-source forward side input terminals VB1, VB2, and VB3, respectively. The capacitor 205 is connected between the floating power-source forward side input terminal VB 1 and the floating power-source negative side input terminal VS 1.
[0068] The capacitor 206 is connected between the floating power-source forward side input terminal VB 2 and the floating power-source negative side input terminal VS 2. The capacitor 207 is connected between the floating power-source forward side input terminal VB 3 and the floating power-source negative side input terminal VS 3. Reference diode 215 is formed in the overvoltage protections of the bottom arm switching element driving signal criteria output terminal VS 0, and is connected between the bottom arm switching element driving signal criteria output terminal VS 0 and the negative side power supply terminal VSS.
[0069] The high proof pressure IC 200 is connected to the inverter circuit of the above-mentioned three phase circuit as follows. That is, three floating power-source negative side input terminals (upper arm switching element driving signal criteria output terminal) VS1, VS2, and VS3 of the high proof pressure IC 200 are connected to each connection nodes E1, E2, and E3 by the side of the upper arm switching element T1, T3, and the emitter of T5, respectively.
[0070] The three upper arm switching element driving signal output terminals UPo, VPo, and WPo are connected to the upper arm switching element T1, T3, each gate G1 of T5, G3, and G5 through gate resistance 208,209,210, respectively. The bottom arm switching element driving signal criteria output

terminal VS 0 is connected to the connection node E0 by the side of the bottom arm switching element T2, T four, and the emitter of T6.

[0071] The bottom arm switching element driving signal output terminals UNo, VNo, and WNo of three pieces are connected to each gates G2, G4, and G6 of the bottom arm switching element T2, T four, and T6 through gate resistance 211,212,213, respectively. The current detection terminal OC is connected to said connection node E0.

[0072] Moreover, the negative side power supply terminal VSS is connected to said connection node N1 of an inverter circuit. Since the current detector 214 is between these connection node E0 and the connection node N1 as mentioned above, the detection electrical potential difference of the current detector 214 will be impressed to the current detection terminal OC.

[0073] Although not illustrated, the parasitism reactor exists in wiring between the bottom arm switching element driving signal criteria output terminal VS 0 and the connection node E0, and especially wiring between the negative side power supply terminal VSS and the connection node N1, respectively.

[0074] Also in the inverter equipment of a three phase circuit shown in drawing 22 , like the case of the single phase inverter equipment shown in drawing 18 , if a high current flows, the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing, respectively between the up-and-down arm switching element driving signal criteria output terminal VS 1, VS0 and VS2, and VS0, VS3 and VS0 will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction.

[0075] Other examples of the common three-phase-circuit inverter equipment it was made to drive the arm switching element of three pairs of upper and lower sides of an inverter circuit with the high proof pressure IC are shown in drawing 23 . The three-phase-circuit inverter circuit of this example is the thing of a configuration of being equivalent to the three-phase-circuit inverter circuit shown in drawing 15 . That is, in eye the 1st phase, antiparallel connection of the up-and-down diodes D1 and D2 is carried out to the switching elements T1 and T2 of a pair with which it comes to connect the emitter of the upper arm switching element T1, and the collector of the bottom arm switching element T2, respectively.

[0076] In eye the 2nd phase, antiparallel connection of the up-and-down diodes D3 and D4 is carried out to switching element T3 of the pair to which it comes to connect the emitter of upper arm switching element T3, and the collector of bottom arm switching element T four, and T four, respectively. In eye the 3rd phase, antiparallel connection of the up-and-down diodes D5 and D6 is carried out to the switching elements T5 and T6 of a pair with which it comes to connect the emitter of the upper arm switching element T5, and the collector of the bottom arm switching element T6, respectively.

[0077] And each Shimo arm switching element T2, T four, and the emitter of T6 are connected to the end of the current detector 214. The other end of the current detector 214 is connected to the external connection terminal N. The anode of each diodes D2, D4, and D6 is connected to the negative side power supply terminal VSS of the high proof pressure IC 200. Common connection of each up arm switching element T1, T3, the collector of T5, and the cathode of each diodes D1, D3, and D5 is made at the external connection terminal P. A driving signal is inputted into each up arm switching element T1, T3, the gate G1 of T5, G3, G5 and each Shimo arm switching element T2, T four, and the gates G2, G4, and G6 of T6 from the high proof pressure IC 200, respectively.

[0078] In addition, about the configuration of others of a three-phase-circuit inverter circuit, the configuration of the high proof pressure IC 200, and connection between an inverter circuit and the high proof pressure IC 200, since it is the same as the thing of a configuration of being shown in drawing 22 , the explanation which attaches the same sign and overlaps is omitted.

[0079] Since the current which flows diodes D2, D4, and D6 does not pass along the current detector 214 by the example of the configuration of this drawing 23 , Although an electrical potential difference does not occur between the connection node E0 and the bottom arm switching element driving signal criteria output terminal VS 0 The seal of approval of the electrical potential difference which is still less than the minimum range of rated pressure-proofing, respectively between the arm switching element

driving signal criteria output terminal VS 1 of the upper and lower sides to the case of a high current drive, VS0 and VS2, and VS0, VS3 and VS0 will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction.

[0080] Moreover, as shown in drawing 24 , the same is said of the case where a current detector is not formed, and the seal of approval of the electrical potential difference which is less than the minimum range of rated pressure-proofing, respectively between the up-and-down arm switching element driving signal criteria output terminal VS 1, VS0 and VS2, and VS0, VS3 and VS0 in a high current drive will be carried out, and the high proof pressure IC 200 will cause proof-pressure destruction. In addition, reference diode 215 is not formed with the inverter equipment of a configuration of being shown in drawing 24 .

[0081]

[Problem(s) to be Solved by the Invention] As mentioned above, with the single phase and the three-phase-circuit inverter equipment which used the conventional high proof pressure IC 100,200 for a switching element drive, there was a trouble that the electrical potential difference exceeding the rated voltage might be built over the high proof pressure IC 100,200, and the high proof pressure IC 100,200 might break by part for few [the bottom arm switching element T2, T four, T6 or diodes D2, D4, and D6, the connection pattern of the current detector 106,214, etc.] inductances at the time of a high current drive.

[0082] This invention was made in order to solve the above-mentioned trouble, and it aims at obtaining the inverter equipment which can prevent the high proof pressure IC for a switching element drive breaking at the time of a high current drive.

[0083]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the inverter equipment concerning this invention connects a clamp diode between the upper arm switching element driving signal criteria output terminal of the high proof pressure IC which drives the switching element of the upper and lower sides of a single phase inverter circuit, and a bottom arm switching element driving signal criteria output terminal.

[0084] According to the inverter equipment concerning this invention, in single phase inverter equipment, the negative electrical potential difference impressed between the upper arm switching element driving signal criteria output terminal of the high proof pressure IC and the bottom arm switching element driving signal criteria output terminal can prevent that it is less than the rated proof-pressure minimum value between those terminals.

[0085] The inverter equipment concerning the next invention connects a clamp diode, respectively between three upper arm switching element driving signal criteria output terminals of the high proof pressure IC which drive the switching element of the upper and lower sides of a three-phase-circuit inverter circuit, and bottom arm switching element driving signal criteria output terminals.

[0086] According to the inverter equipment concerning this invention, in three-phase-circuit inverter equipment, the negative electrical potential difference impressed, respectively between three upper arm switching element driving signal criteria output terminals of the high proof pressure IC and bottom arm switching element driving signal criteria output terminals can prevent that it is less than the rated proof-pressure minimum value between those terminals.

[0087] The inverter equipment concerning the next invention uses a clamp diode as the external components of the high proof pressure IC.

[0088] According to the inverter equipment concerning this invention, while the design change of the high proof pressure IC is unnecessary, this invention is applicable also to the inverter equipment which used the existing high proof pressure IC.

[0089] The inverter equipment concerning the next invention forms the means of communication which transmits the signal which operates according to the independent power source other than the drive power source of the high proof pressure IC which drives the switching element of the upper and lower sides of the inverter circuit which has a current detection means, and is outputted from a current detection means to the high proof pressure IC.

[0090] Since potential of a negative side power supply terminal and a bottom arm switching element driving signal criteria output terminal can be made equal by having established a means to transmit the output from a current detector to the high proof pressure IC according to the inverter equipment concerning this invention, it is prevented that a negative electrical potential difference is impressed with the circuit pattern of a current detector etc. between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.
[0091] The inverter equipment concerning the next invention constitutes a means of communication with an operational amplifier, and uses it as the external components of the high proof pressure IC.
[0092] According to the inverter equipment concerning this invention, while the design change of the high proof pressure IC is unnecessary, this invention is applicable also to the inverter equipment which used the existing high proof pressure IC.
[0093] The inverter equipment concerning the next invention connects to the anode of the diode of a bottom arm wiring connected to the bottom arm switching element driving signal criteria output terminal while connecting wiring connected to the upper arm switching element driving signal criteria output terminal of the high proof pressure IC which drives the switching element of the upper and lower sides of a single phase inverter circuit near the cathode of the diode of a bottom arm.
[0094] In not forming a current detector according to the inverter equipment concerning this invention It is lost by the amount of [by the inductance produced with the conventional circuit pattern] electrical-potential-difference generating. Since the negative electrical potential difference which may be impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal turns into only ON state voltage of the diode of a bottom arm mostly It is prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal. If the negative electrical potential difference generated by the current detector between up-and-down arm switching element driving signal criteria output terminals is low when a current detector is formed, it will be prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.
[0095] The inverter equipment concerning the next invention prepares the bonding pad of dedication by which the other end of wiring by which the end was connected to the bottom arm switching element driving signal criteria output terminal was connected to the three-phase-circuit inverter circuit part. The high proof pressure IC which drives the switching element of the upper and lower sides of a three-phase-circuit inverter circuit While connecting three wiring connected to three upper arm switching element driving signal criteria output terminals, respectively near the cathode of the diode of the bottom arm of three, respectively The bonding pad of said dedication and the anode of the diode of the bottom arm of three are electrically connected with a wire, respectively.
[0096] According to the inverter equipment concerning this invention, it sets to three-phase-circuit inverter equipment. While the current which becomes main for each wiring path which results in each up arm switching element driving signal criteria output terminal of the high proof pressure IC from each cathode of 3 diodes of a bottom arm flows Since the current which becomes main also for each wiring path which results in each Shimo arm switching element driving signal criteria output terminal of the high proof pressure IC from each anode of three diodes of a bottom arm flows Since the negative electrical potential difference which may be impressed between three upper arm switching element driving signal criteria output terminals and bottom arm switching element driving signal criteria output terminals turns into only ON state voltage of the diode of the bottom arm of about three, respectively in not forming a current detector It is prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between three upper arm switching element driving signal criteria output terminals and bottom arm switching element driving signal criteria output terminals. If each negative electrical potential difference generated by the current detector between up-and-down arm switching element driving signal criteria output terminals is low when a current detector

is formed, it will be prevented that a less [than the rated proof-pressure minimum value] negative electrical potential difference is impressed between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal.

[0097] The diode with larger current capacity as diode of the bottom arm of the inverter circuit driven with the high proof pressure IC than the diode of other switching elements and an upper arm is used for the inverter equipment concerning the next invention.

[0098] Since the ON state voltage of the diode of the bottom arm which is one of the causes of destructive of the high proof pressure IC when only the diode of a bottom arm uses what has large current capacity can be stopped low according to the inverter equipment concerning this invention, the margin to proof-pressure destruction of the high proof pressure IC becomes so large.

[0099]

[Embodiment of the Invention]

(Gestalt 1 of operation) Drawing 1 is the schematic diagram showing an example of the single phase inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 1 of this operation to drawing 18 A clamp diode 110 is connected between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Only when the electrical potential difference V between the criteria output terminals VS [VS1 and] 0 of these upper and lower sides (VS1-VS0) turns into a negative electrical potential difference, a clamp diode 110 turns on and the electrical potential difference V (VS1-VS0) is maintained at the ON state voltage of a clamp diode 110.

[0100] In drawing 1 T1 and T2, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1 and D2 was carried out to the upper arm switching element T1 and the bottom arm switching element T2, respectively, G1 and G2, respectively The gate of the upper arm switching element T1 and the bottom arm switching element T2, The resistance to which 104 and 105 were connected to each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2, respectively, They are the DC power supply which a current detector becomes in 106 and the reactor as a load and 108 become from power-source body 108a and capacitor 108b in 107.

[0101] E1 and E0 Moreover, the connection node by the side of each emitter of the upper arm switching element T1 and the bottom arm switching element T2, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, The reactor with which the output terminal of an inverter circuit, L1, L2, L3, L4 and L5, L6, and L7 are [U] parasitic on a wiring part, and I1, I2 and I3 are the current which flows the upper arm switching element T1, the current which flows to diode D2, and a current which flows a reactor 107, respectively. The current detector 106 is formed on the bus-bar with which common connection of the emitter of the bottom arm switching element T2 and the anode of diode D2 was made.

[0102] In drawing 1 100 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 101 supplies driver voltage to the high proof pressure IC 100, and 102 Diode, As for a capacitor and 109, reference diode, and a1, a2, a3, a4, a5 and a6 is [103] the circuit blocks inside the high proof pressure IC 100. As for the bottom arm side driver circuit where the upper arm side driver circuit where an input buffer and a2 drive a level shifter, and, as for a3, a1 drives the upper arm switching element T1, and a4 drive the bottom arm switching element T2, and a5, an overcurrent detector and a6 are error signal generators.

[0103] Moreover, UPi, UNi, UPo, UNo, VB1, VS1, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 100. The upper arm switching element driving signal output terminal to which UPi and UNi output a driving signal input terminal, and UPo outputs the driving signal of the upper arm switching element T1, respectively, The bottom arm switching element driving signal output terminal to which UNo outputs the driving signal of the bottom arm switching element T2, While VB1 is a floating power-source forward side input terminal and VS1 is a floating power-source

negative side input terminal, an upper arm switching element driving signal criteria output terminal, For VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.

[0104] In the configuration of the inverter equipment shown in drawing 1 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 18 .

[0105] By the way, generally the minimum value of pressure-proofing of the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent. That is, the rated proof-pressure minimum value of the electrical potential difference V between the arm switching element driving signal criteria output terminals VS [VS1 and] 0 of the upper and lower sides of the high proof pressure IC 100 (VS1-VS0) is abbreviation-5V.

[0106] Therefore, especially in the gestalt 1 of this operation, as said clamp diode 110, although not limited, the common diode whose ON state voltage is about 0.7V-2V, for example is used. Then, when a negative electrical potential difference is built between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, the electrical potential difference between them is clamped by the ON state voltage of a clamp diode 110, i.e., about -0.7V--2V. In addition, it is good to form a clamp diode 110 immediately near the criteria output terminals VS0 and VS1 of the high proof pressure IC 100 preferably, and to stop as short as possible the wire length from these terminals VS0 and VS1 to a clamp diode 110.

[0107] An operation of the inverter equipment of a configuration of being shown in drawing 1 is explained. Only when the seal of approval of the negative electrical potential difference which can become the cause of making this IC100 destroying between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 is carried out, a clamp diode 110 serves as ON and clamps the electrical potential difference V between these terminals VS [VS1 and] 0 (VS1-VS0) to ON state voltage (about 0.7V-2V). Therefore, an electrical potential difference V (VS1-VS0) becomes about -0.7V--2V, and is not less than rated proof-pressure minimum value-5V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100.

[0108] As explained above, according to the gestalt 1 of this operation The electrical potential difference V between terminals (VS1-VS0) when a negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 becomes about -0.7V--2V. Since it can prevent that it is less than rated proof-pressure minimum value-5V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0109] In addition, the anode of diode D2 is connected to the direct negative side power supply terminal VSS like the single phase inverter equipment shown in drawing 2 , without minding the current detector 106. Also in the inverter equipment of a configuration of that only the emitter of the bottom arm switching element T2 is shown in drawing 20 linked to the current detector 106 A clamp diode 110 can be formed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential difference V between these terminals VS [VS1 and] 0 of the high proof pressure IC 100 (VS1-VS0) is less than rated proof-pressure minimum value-5V, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0110] Moreover, also in the inverter equipment of a configuration of being shown in drawing 21 it was made not to form a current detector like the single phase inverter equipment shown in drawing 3 , a clamp diode 110 can be formed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential difference V

between these terminals VS [VS1 and] 0 of the high proof pressure IC 100 (VS1-VS0) is less than rated proof-pressure minimum value-5V, proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0111] (Gestalt 2 of operation) Drawing 4 is the schematic diagram showing an example of the three-phase-circuit inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 2 of this operation to drawing 22 Between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminals VS 0, Between the upper arm switching element driving signal criteria output terminal VS 2 and the bottom arm switching element driving signal criteria output terminals VS 0, A clamp diode 216,217,218 is connected, respectively between the upper arm switching element driving signal criteria output terminal VS 3 and the bottom arm switching element driving signal criteria output terminal VS 0.

[0112] And each electrical potential difference V between each upper criteria output terminals VS1, VS2, and VS3 and the lower criteria output terminal VS 0 (VS1-VS0) Only when V (VS2-VS0) and V (VS3-VS0) become a negative electrical potential difference, respectively, the clamp diode 216,217,218 turns on. Each electrical potential difference V (VS1-VS0) V (VS2-VS0) and V (VS3-VS0) are maintained at the ON-state voltage of a clamp diode 216,217,218, respectively.

[0113] In drawing 4 T1, T3, T5 and T2, T four, and T6, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1, D3, D5, and D2, D4 and D6 was carried out to the upper arm switching element T1, T3, T5 and the bottom arm switching element T2, T four, and T6, respectively, G1, G3, G5, and G2, G4 and G6 are the upper arm switching element T1, T3, T5 and the bottom arm switching element T2, T four, and the gate of T6, respectively.

[0114] The resistance by which 208,209,210 and 211,212,213 were connected to the upper arm switching element T1, T3, the gate G1 of T5, G3, G5 and the bottom arm switching element T2, T four, and the gates G2, G4, and G6 of T6, respectively, and 214 Moreover, a current detector, E1, E2, and E3, respectively The upper arm switching element T1, T3, the connection node by the side of the emitter of T5, The connection node the bottom arm switching element T2, T four, and by the side of each emitter of T6 with common E0, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, and U, V and W are the output terminals of the inverter circuit of each three phase circuit, respectively. The current detector 214 is formed on each Shimo arm switching element T2, T four, and the bus-bar with which common connection of the emitter of T6 and the anode of each diodes D2, D4, and D6 was made.

[0115] In drawing 4 200 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 201 supplies driver voltage to the high proof pressure IC 200, and 202,203,204 Diode, A capacitor and 215 205,206,207 Reference diode, b1, b2, b3, b4, b5, b6, b7, b8, b9, b10, b11, and b12 are the circuit blocks inside the high proof pressure IC 200. The upper arm side driver circuit where an input buffer, and b2, b3 and b4 drive a level shifter, and, as for b5, b6, and b7, b1 drives the upper arm switching element T1, T3, and T5, respectively, As for the bottom arm side driver circuit where b8, b9, and b10 drive the bottom arm switching element T2, T four, and T6, respectively, and b11, an overcurrent detector and b12 are error signal generators.

[0116] Moreover, UPi, UNi, VPi, VNi, WPi, WNi, UPo, VPo, WPo, UNo, VNo, WNo, VB1, VB2, VB3, VS1, VS2, VS3, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 200. UPi, VPi, WPi, and UNi, VNi and WNi, respectively A driving signal input terminal, The upper arm switching element driving signal output terminal to which UPo, VPo, and WPo output the upper arm switching element T1, T3, and the driving signal of T5, respectively, The bottom arm switching element driving signal output terminal to which UNo, VNo, and WNo output the bottom arm switching element T2, T four, and the driving signal of T6, respectively, While VB1, VB2, and VB3 are floating power-source negative side input terminals, a floating power-source forward side input terminal, and VS1, VS2 and VS3 An upper arm switching element driving signal criteria output terminal, For

VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.
[0117] In the configuration of the inverter equipment shown in drawing 4 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 22 .
[0118] Here, generally the minimum value of each pressure-proofing of the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 is [(potential of bottom arm switching element driving signal criteria output terminal VS 0) -5] bolt extent as the gestalt 1 of operation explained. That is, the rated proof-pressure minimum value of the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 and the bottom arm switching element driving signal criteria output terminal VS 0 is abbreviation-5V, respectively.
 [0119] Therefore, especially in the gestalt 2 of this operation, as said clamp diode 216,217,218, although not limited, the common diode whose ON state voltage is about 0.7V-2V, for example is used. Then, when a negative electrical potential difference is built between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 and the bottom arm switching element driving signal criteria output terminal VS 0, the electrical potential difference between them is clamped by the ON state voltage of a clamp diode 216,217,218, i.e., about -0.7V--2V.
[0120] In addition, it is good to form each clamp diode 216,217,218 immediately the criteria output terminal VS 0 of the high proof pressure IC 200, and near VS1, VS2, and VS3 preferably, and to stop as short as possible these terminals VS 0 and the wire length from VS1, VS2, and VS3 to each clamp diode 216,217,218.
[0121] An operation of the inverter equipment of a configuration of being shown in drawing 4 is explained. Between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 Only when the seal of approval of the negative electrical potential difference which can become the cause of making this IC200 destroying is carried out A clamp diode 216,217,218 serves as ON and clamps the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS1, VS2, VS3, and VS0 to ON state voltage (about 0.7V-2V), respectively. Therefore, electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) become about -0.7V--2V, respectively, and are not less than rated proof-pressure minimum value-5V between these terminals VS1, VS2, VS3, and VS0 of the high proof pressure IC 200.
[0122] As explained above, according to the gestalt 2 of this operation The electrical potential difference V between terminals when a negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 (VS1-VS0) Since it can prevent that V (VS2-VS0) and V (VS3-VS0) become about -0.7V--2V, respectively, and it is less than rated proof-pressure minimum value-5V between these terminals VS1, VS2, VS3, and VS0 of the high proof pressure IC 200 Proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0123] In addition, the anode of each diodes D2, D4, and D6 is connected to the direct negative side power supply terminal VSS like the three-phase-circuit inverter equipment shown in drawing 5 , without minding the current detector 214. Also in each Shimo arm switching element T2, T four, and the inverter equipment of a configuration of that only the emitter of T6 is shown in drawing 23 linked to the current detector 214 A clamp diode 216,217,218 can be formed, respectively between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS [VS1 VS2, VS3, and] 0 of the high proof pressure IC 200 are less than rated proof-pressure minimum value-5V, respectively, proof-pressure destruction of the high proof pressure IC 200

can be prevented.
[0124] Moreover, also in the inverter equipment of a configuration of being shown in drawing 24 it was made not to form a current detector like the three-phase-circuit inverter equipment shown in drawing 6 , a clamp diode 216,217,218 can be formed, respectively between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0. Then, since it can prevent that the electrical potential differences V (VS1-VS0), V (VS2-VS0), and V (VS3-VS0) between these terminals VS [VS1 VS2, VS3, and] 0 of the high proof pressure IC 200 are less than rated proof-pressure minimum value-5V, respectively, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0125] (Gestalt 3 of operation) Drawing 7 is the schematic diagram showing an example of the single phase inverter equipment which applied this invention. In the common inverter equipment which shows the inverter equipment of the gestalt 3 of this operation to drawing 18 Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 106 to the high proof pressure IC 100 is formed. By connecting the negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0, and making it same electric potential It prevents building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0.
[0126] In drawing 7 T1 and T2, respectively An upper arm switching element and a bottom arm switching element, The diode with which antiparallel connection of D1 and D2 was carried out to the upper arm switching element T1 and the bottom arm switching element T2, respectively, G1 and G2, respectively The gate of the upper arm switching element T1 and the bottom arm switching element T2, The resistance to which 104 and 105 were connected to each gates G1 and G2 of the upper arm switching element T1 and the bottom arm switching element T2, respectively, They are the DC power supply which a current detector becomes in 106 and the reactor as a load and 108 become from power-source body 108a and capacitor 108b in 107.
[0127] E1 and E0 Moreover, the connection node by the side of each emitter of the upper arm switching element T1 and the bottom arm switching element T2, N1 sandwiches the current detector 106. With the connection node E0 The connection node of the opposite side, The power supply terminal with which P impresses forward supply voltage to an inverter circuit, the power supply terminal with which N impresses negative supply voltage to an inverter circuit, The reactor with which the output terminal of an inverter circuit, L1, L2, L3, L4 and L5, and L6 are [U] parasitic on a wiring part, and I1, I2 and I3 are the current which flows the upper arm switching element T1, the current which flows to diode D2, and a current which flows a reactor 107, respectively. The current detector 106 is formed on the bus-bar with which common connection of the emitter of the bottom arm switching element T2 and the anode of diode D2 was made.
[0128] In drawing 7 100 Moreover, the high proof pressure IC for a switching element drive of an inverter circuit The external power by which 101 supplies driver voltage to the high proof pressure IC 100, and 102 Diode, 103 is a capacitor and a1, a2, a3, a4, a5, and a6 are the circuit blocks inside the high proof pressure IC 100. As for the bottom arm side driver circuit where the upper arm side driver circuit where an input buffer and a2 drive a level shifter, and, as for a3, a1 drives the upper arm switching element T1, and a4 drive the bottom arm switching element T2, and a5, an overcurrent detector and a6 are error signal generators.
[0129] Moreover, UPi, UNi, UPo, UNo, VB1, VS1, VS0, OC, Fo, VCC, and VSS are the input/output terminals of the high proof pressure IC 100. The upper arm switching element driving signal output terminal to which UPi and UNi output a driving signal input terminal, and UPo outputs the driving signal of the upper arm switching element T1, respectively, The bottom arm switching element driving signal output terminal to which UNo outputs the driving signal of the bottom arm switching element T2, While VB1 is a floating power-source forward side input terminal and VS1 is a floating power-source

negative side input terminal, an upper arm switching element driving signal criteria output terminal, For VS0, a bottom arm switching element driving signal criteria output terminal and OC are [an error output terminal, and VCC and VSS of a current detection terminal and Fo] a forward side and the power supply terminal of a negative side, respectively.

[0130] In the configuration of the inverter equipment shown in drawing 7 , the explanation which attaches the same sign and overlaps is omitted about the same configuration as the inverter equipment shown in drawing 18 .

[0131] The operational amplifier 111 has negative supply with the another high proof pressure IC 100, the forward side input terminal is connected to the connection node E0 near the emitter of the bottom arm switching element T2, and the negative side input terminal is connected to the connection node N1. The output terminal of an operational amplifier 111 is connected to the overcurrent detector a5 through the current detection terminal OC of the high proof pressure IC 100.

[0132] The anode of the clamp diode 114 which prevents building a negative electrical potential difference over this terminal OC is connected to the current detection terminal OC. The cathode of the clamp diode 114 is connected to the grounding point. In addition, since a clamp diode 114 only clamps the output of an operational amplifier 111, it is good for the diode for small signals.

[0133] Preferably, it is good to connect the negative side power supply terminal VSS of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0 immediately near the high proof pressure IC 100.

[0134] An operation of the inverter equipment of a configuration of being shown in drawing 7 is explained. Usually, since the potential difference to which the polar electrical-potential-difference E0, i.e., connection node, side as shown in the current detector 106 by "+" and "-" at drawing 7 becomes higher than the connection node N1 side occurs, it is reversed with an operational amplifier 111 and a forward electrical potential difference is impressed to the current detection terminal OC. Since the operational amplifier 111 has the negative electrical potential difference when a current is intercepted and induction of the negative electrical potential difference is carried out by few wiring inductances, as explained in the above-mentioned conventional technique, if it is electrical-potential-difference within the limits of the negative electrical potential difference, an operational amplifier 111 will not break. Although the negative electrical potential difference outputted from the operational amplifier 111 will be impressed to the current detection terminal OC of the high proof pressure IC in that case, since the potential of the current detection terminal OC is clamped by the clamp diode 114, the high proof pressure IC 100 does not destroy it.

[0135] By having established a means to transmit the output from the current detector 106 to the high proof pressure IC 100 according to the gestalt 3 of this operation, as explained above Since potential of the negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 can be made equal It can prevent impressing a negative electrical potential difference with the circuit pattern of the current detector 106 etc. between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, and proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0136] In addition, like the single phase inverter equipment shown in drawing 8 , as the current detector 106 is not minded for the anode of diode D2, only the emitter of the bottom arm switching element T2 is also set to the inverter equipment of a configuration of being shown in drawing 20 linked to the current detector 106. Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 106 to the high proof pressure IC 100 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 100

can be prevented.
[0137] Moreover, it also sets to the inverter equipment of a configuration of being shown in drawing 22 which comes to prepare the current detector 214 like the three-phase-circuit inverter equipment shown in drawing 9 on each Shimo arm switching element T2, T four, and the bus-bar with which common connection of the emitter of T6 and the anode of each diodes D2, D4, and D6 was made. Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 214 to the high proof pressure IC 200 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential.
[0138] Moreover, for the current detection terminal OC, it clamps with a clamp diode 114. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0139] Furthermore, the ** which does not connect the anode of each diodes D2, D4, and D6 to the current detector 214 like the three-phase-circuit inverter equipment shown in drawing 10 , Also in each Shimo arm switching element T2, T four, and the inverter equipment of a configuration of that only the emitter of T6 is shown in drawing 23 which it comes to connect with the current detector 214 Connect with an operational amplifier 111 and the resistance 112,113 which determines an operational amplifier 111 and the gain of the operational amplifier 111 as means of signal communication which transmit the signal of the current detector 214 to the high proof pressure IC 200 is formed. The negative side power supply terminal VSS and the bottom arm switching element driving signal criteria output terminal VS 0 are connected, and it may be made to make it same electric potential.
[0140] Moreover, for the current detection terminal OC, it clamps with a clamp diode 114. Then, since it can prevent building a negative electrical potential difference between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0141] Although the operational amplifier 111 was used with the gestalt 3 of the above-mentioned implementation further again as a means to transmit the output of the current detector 106,214 to the high proof pressure IC 100,200, the same effectiveness is acquired, even if it replaces with an operational amplifier 111 and uses insulating amplifier, an analog photo coupler, etc.
[0142] (Gestalt 4 of operation) Drawing 11 is the mimetic diagram showing the example of chip arrangement of the inverter circuit in the single phase inverter equipment concerning this invention. This inverter circuit The chip of the upper arm switching element T1 The chip of diode D1 by which antiparallel connection was carried out to 301 and the upper arm switching element T1 (An upper arm switching element chip is called hereafter) The chip of 302 and the bottom arm switching element T2 (An upper arm diode chip is called hereafter) The chip of diode D2 by which antiparallel connection was carried out to 303 and the bottom arm switching element T2 (A bottom arm switching element chip is called hereafter) The bonding pad used as the power supply terminal P which impresses forward supply voltage to 304 and an inverter circuit (A bottom arm diode chip is called hereafter) (In the gestalt 4 of this operation, it considers as a bonding pad P hereafter) It has composition equipped with the bonding pad (it considers as a bonding pad N similarly hereafter) used as the power supply terminal N which impresses negative supply voltage to an inverter circuit, and the bonding pad (it considers as a bonding pad U similarly hereafter) used as the output terminal U of an inverter circuit.
[0143] Gate 301G (field surrounded squarely) are prepared in a part of the front face, and the upper arm switching element chip 301 is formed so that chip front faces other than the field which is gate 301G may serve as collector 301C. The rear face of the upper arm switching element chip 301 is emitter 301E. Collector 301C of the upper arm switching element T1 is directly in contact with the bonding pad P.
[0144] Emitter 301E of the upper arm switching element T1 is electrically connected to the bonding pad U through the wire W1. Although not limited especially, in drawing 11 , the wire W1 serves as a wire bundle which consists of three wires. Gate 301G of the upper arm switching element T1 are electrically

connected to the upper arm switching element driving signal output terminal UPo of the high proof pressure IC 100 (omitted in drawing 11) through the bonding wire W2.
[0145] By anode 302A, the front face is formed by the upper arm diode chip 302 so that a rear face may serve as cathode 302C. Cathode 302C of diode D1 is directly in contact with the bonding pad P, and anode 302A is electrically connected to the bonding pad U through wire W3. Although not limited especially, in drawing 11 , wire W3 serves as a wire bundle which consists of three wires.
[0146] Gate 303G (field surrounded squarely) are prepared in a part of the front face, and the bottom arm switching element chip 303 is formed so that chip front faces other than the field which is gate 303G may serve as collector 303C. The rear face of the bottom arm switching element chip 303 is emitter 303E. Collector 303C of the bottom arm switching element T2 is directly in contact with the bonding pad U.
[0147] Emitter 303E of the bottom arm switching element T2 is electrically connected to the bonding pad N through the wire W4. Although not limited especially, in drawing 11 , the wire W4 serves as a wire bundle which consists of three wires. Gate 303G of the bottom arm switching element T2 are electrically connected to the bottom arm switching element driving signal output terminal UNo of the high proof pressure IC 100 (omitted in drawing 11) through the bonding wire W5.
[0148] By anode 304A, the front face is formed by the bottom arm diode chip 304 so that a rear face may serve as cathode 304C. Cathode 304C of diode D2 is directly in contact with the bonding pad U, and anode 304A is electrically connected to the bonding pad N through the wire W6. Although not limited especially, in drawing 11 , the wire W6 serves as a wire bundle which consists of three wires.
[0149] Moreover, anode 304A of the bottom arm diode chip 304 is electrically connected to the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 100 (illustration abbreviation) through the bonding wire W7. Near the bottom arm diode chip 304 of a bonding pad U, the bonding wire W7 connected to the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 (illustration abbreviation) is connected electrically.
[0150] The circuit diagram of the inverter circuit of a configuration of being shown in drawing 11 is shown in drawing 12 . The wiring section which attached hatching in drawing 12 is the bonding pad of Above P, U, and N, and the wiring section shown as the continuous line is a bonding wire. According to the configuration shown in drawing 11 , it turns out that the bonding wire W8 which the bonding wire W7 connected to the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 100 (illustration abbreviation) from anode 304A of diode D2 was pulled out, and was connected to the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 (illustration abbreviation) near cathode 304C of diode D2 is pulled out so that clearly from this drawing.
[0151] In addition, in drawing 11 and drawing 12 , the wiring section which attached signs X1 and X0, and was shown with the broken line is a bonding wire with which connection with the arm switching element driving signal criteria output terminals VS1 and VS0 of the upper and lower sides in the conventional inverter circuit is presented, respectively.
[0152] Since according to the gestalt 4 of this operation a bonding wire W7 is connected to anode 304A of diode D2 and the bonding wire W8 is connected near cathode 304C of diode D2, as explained above, In not forming a current detector, the amount of [by the inductances La and Lb (refer to drawing 12) produced with the conventional circuit pattern] electrical-potential-difference generating loses. The negative electrical potential difference which may be impressed between the upper arm switching element driving signal criteria output terminal VS 1 and the bottom arm switching element driving signal criteria output terminal VS 0 is ON state voltage VF (usually) of diode D2 mostly. It is prevented that a less [than rated proof-pressure minimum value-5V] negative electrical potential difference is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100 and the bottom arm switching element driving signal criteria output terminal VS 0 since it becomes. even if high -- about 3V -- it is only -- Proof-pressure destruction of the high proof pressure IC 100 can be prevented.

[0153] moreover, when the current detector 106 is formed according to the gestalt 4 of this operation Although the negative electrical potential difference by various factors which were explained with the above-mentioned conventional technique besides ON-state-voltage VF of diode D2 occurs and is impressed between the upper arm switching element driving signal criteria output terminal VS 1 of the high proof pressure IC 100, and the bottom arm switching element driving signal criteria output terminal VS 0 Since it decreases about a part for electrical-potential-difference generating by the inductances La and Lb (refer to drawing 12) produced with the conventional circuit pattern If the negative electrical potential difference generated by the current detector 106 among the up-and-down arm switching element driving signal criteria output terminals VS [VS1 and] 0 is low, proof-pressure destruction of the high proof pressure IC 100 can be prevented.
[0154] (Gestalt 5 of operation) Drawing 13 is the mimetic diagram showing the example of chip arrangement of the inverter circuit when not forming the current detector of the three-phase-circuit inverter equipment concerning this invention.
[0155] This inverter circuit Each chip of the upper arm switching element T1, T3, and T5 Each chip of diodes D1, D3, and D5 by which antiparallel connection was carried out to 401,402,403 and the upper arm switching element T1, T3, and T5, respectively (An upper arm switching element chip is called hereafter) Each chip of 407,408,409, the bottom arm switching element T2, T four, and T6 (An upper arm diode chip is called hereafter) Each chip of diodes D2, D4, and D6 by which antiparallel connection was carried out to 404,405,406 and the bottom arm switching element T2, T four, and T6, respectively (A bottom arm switching element chip is called hereafter) The bonding pad used as the power supply terminal P which impresses forward supply voltage to 410,411,412 and an inverter circuit (A bottom arm diode chip is called hereafter) (In the gestalt 5 of this operation, it considers as a bonding pad P hereafter) The bonding pad used as the power supply terminal N which impresses negative supply voltage to an inverter circuit Each bonding pad used as the output terminals U, V, and W of (it considers as a bonding pad N similarly hereafter), and an inverter circuit The bonding pad of dedication to which the bonding wire W10 connected to the bottom arm switching element driving signal criteria output terminal VS 0 (which it lets hereafter be bonding pads U, V, and W similarly, respectively) is connected electrically (The bonding pad for VS0 is called hereafter) It has composition equipped with 420.
[0156] Gates 401G, 402G, and 403G (field surrounded squarely) are established in a part of the front face, respectively, and the upper arm switching element chip 401,402,403 is formed so that chip front faces other than the field which are each gates 401G, 402G, and 403G may serve as Collectors 401C, 402C, and 403C, respectively. The rear face of each up arm switching element chip 401,402,403 serves as Emitters 401E, 402E, and 403E, respectively. Each up arm switching element T1, T3, and the collectors 401C, 402C, and 403C of T5 are directly in contact with the bonding pad P. Each up arm switching element T1, T3, and the emitters 401E, 402E, and 403E of T5 are electrically connected to the bonding pad U through wires W11, W12, and W13, respectively.
[0157] Although not limited especially, in drawing 13 , wires W11, W12, and W13 serve as a wire bundle which all consists of three wires. Each up arm switching element T1, T3, and the gates 401G, 402G, and 403G of T5 are electrically connected to the upper arm switching element driving signal output terminals UPo, VPo, and WPo of the high proof pressure IC 200 (illustration abbreviation) through the bonding wire (illustration abbreviation), respectively.
[0158] With Anodes 407A, 408A, and 409A, each front face is formed by the upper arm diode chip 407,408,409 so that each rear face may serve as Cathodes 407C, 408C, and 409C. The cathodes 407C, 408C, and 409C of each diodes D1, D3, and D5 are directly in contact with the bonding pad P, and Anodes 407A, 408A, and 409A are electrically connected to the bonding pad U through wires W14, W15, and W16. Although not limited especially, in drawing 13 , each of wires W14, and 15 and 16 is the wire bundle which consists of three wires.
[0159] Gates 404G, 405G, and 406G (field surrounded squarely) are established in a part of each front face, and the bottom arm switching element chip 404,405,406 is formed so that chip front faces other than the field which are each gates 404G, 405G, and 406G may serve as Collectors 404C, 405C, and 406C, respectively. The rear face of each Shimo arm switching element chip 404,405,406 serves as

Emitters 404E, 405E, and 406E, respectively.
[0160] Each Shimo arm switching element T2, T four, and the collectors 404C, 405C, and 406C of T6 are directly in contact with the bonding pad U. Each Shimo arm switching element T2, T four, and the emitters 404E, 405E, and 406E of T6 are electrically connected to the bonding pad N through wires W17, W18, and W19, respectively. Although not limited especially, in drawing 13 , wires W17, W18, and W19 serve as a wire bundle which all consists of three wires. Each Shimo arm switching element T2, T four, and the gates 404G, 405G, and 406G of T6 are electrically connected to the bottom arm switching element driving signal output terminals UNo, VNo, and WNo of the high proof pressure IC 200 (illustration abbreviation) through the bonding wire (illustration abbreviation), respectively.
[0161] With Anodes 410A, 411A, and 412A, each front face is formed by the bottom arm diode chip 410,411,412 so that each rear face may serve as Cathodes 410C, 411C, and 412C. The cathodes 410C, 411C, and 412C of each diodes D2, D4, and D6 are directly in contact with the bonding pad U, and Anodes 410A, 411A, and 412A are electrically connected to the bonding pad N through wires W20, W21, and W22. Although not limited especially, in drawing 13 , each of wires W20, and 21 and 22 is the wire bundle which consists of three wires.
[0162] Moreover, the anodes 410A, 411A, and 412A of each Shimo arm diode chip 410,411,412 are electrically connected to the bonding pad 420 for VS0 through a bonding wire W23, and 24 and 25, respectively.
[0163] Furthermore, each bonding pads U, V, and W are electrically connected to the wiring section 421,422,423 by which pattern shaping was carried out through bonding wires W26, W27, and W28 near the bottom arm diode chip 410,411,412, respectively. Each wiring section 421,422,423 is electrically connected to the upper arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 (illustration abbreviation) through a bonding wire W29, and 30 and 31, respectively.
[0164] As explained above, according to the gestalt 5 of this operation While the current which becomes main for the wiring path which results in each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200 from the cathodes 410C, 411C, and 412C of each diodes D2, D4, and D6 of a bottom arm flows Since the current which becomes main also for the wiring path which results in the bottom arm switching element driving signal criteria output terminal VS 0 of the high proof pressure IC 200 from the anodes 410A, 411A, and 412A of each diodes D2, D4, and D6 flows The electrical potential difference V impressed among the arm switching element driving signal criteria output terminals VS1, VS2, VS3, and VS0 of these upper and lower sides (VS1-VS0) V (VS2-VS0) and V (VS3-VS0) become only ON state voltage VF of each diodes D2, D4, and D6, and can prevent proof-pressure destruction of the high proof pressure IC 200.
[0165] moreover, when the current detector 214 is formed according to the gestalt 5 of this operation Between each up arm switching element driving signal criteria output terminals VS1, VS2, and VS3 of the high proof pressure IC 200, and the bottom arm switching element driving signal criteria output terminal VS 0 Although the negative electrical potential difference by various factors which were explained with the above-mentioned conventional technique besides ON-state-voltage VF of diodes D2, D4, and D6 occurs and is impressed Since it decreases about a part for electrical-potential-difference generating by the inductance produced with the conventional circuit pattern If the negative electrical potential difference generated by the current detector 214 among the up-and-down arm switching element driving signal criteria output terminals VS1, VS2, VS3, and VS0 is low, proof-pressure destruction of the high proof pressure IC 200 can be prevented.
[0166] (Gestalt 6 of operation) Next, the gestalt 6 of operation concerning this invention is explained. The description of the gestalt 6 of this operation is using what has larger current capacity than the switching element and diode of others [diode] by which antiparallel connection's was carried out to the bottom arm switching element among two or more switching elements and diodes which are used for the inverter circuit. That is, it is because ON state voltage VF of this diode will become low and the negative electrical potential difference impressed between the arm switching element driving signal criteria output terminals of the upper and lower sides of the high proof pressure IC will become smaller,

if the current capacity of the diode of a bottom arm becomes large.
[0167] An example of the electrical-potential-difference VF and the current IF property of the diode used for inverter equipment is shown in drawing 14 . Generally, in the time of an output short circuit etc., a current may flow a 300A grade. In such a case, as shown in drawing 14 , for the diode of 50A, ON state voltage VF will be set to 5V, and current capacity will reach the rated voltage of the high proof pressure IC only by it. however, current capacity -- the diode of 75A -- the ON state voltage -- about 3.5 -- in order to end by V, it comes out so much and the quantity proof pressure IC is not destroyed In addition, in the conventional inverter circuit, the diodes of a bottom arm were also other switching elements and the thing of the same current capacity as diode.
[0168] Therefore, since ON state voltage VF of the diode of the bottom arm which is one of the causes of destructive of the high proof pressure IC when only the diode of a bottom arm uses what has large current capacity can be stopped low according to the gestalt 7 of operation, the margin to proof-pressure destruction of the high proof pressure IC becomes large, and it is hard coming to destroy the high proof pressure IC.
[0169] In addition, it cannot be overemphasized that the current capacity of the diode of a bottom arm is not restricted to 75A.
[0170]
[Effect of the Invention] As mentioned above, since it can prevent that the negative electrical potential difference impressed between the upper arm switching element driving signal criteria output terminal of the high proof pressure IC and the bottom arm switching element driving signal criteria output terminal is less than the rated proof-pressure minimum value between those terminals in single phase inverter equipment according to the inverter equipment concerning this invention as explained, proof-pressure destruction of the high proof pressure IC can be prevented.
[0171] Since it can prevent that the negative electrical potential difference impressed, respectively between three upper arm switching element driving signal criteria output terminals of the high proof pressure IC and bottom arm switching element driving signal criteria output terminals is less than the rated proof-pressure minimum value between those terminals in three-phase-circuit inverter equipment according to the inverter equipment concerning the next invention, proof-pressure destruction of the high proof pressure IC can be prevented.
[0172] Since the design change of the high proof pressure IC is unnecessary, while according to the inverter equipment concerning the next invention being able to prevent destruction of the high proof pressure IC besides the above-mentioned effectiveness as the cost which hardly changes to the former is also, this invention can be applied also to the inverter equipment which used the existing high proof pressure IC, and the effectiveness that destruction of the high proof pressure IC of existing equipment can be prevented is acquired.
[0173] Since potential of a negative side power supply terminal and a bottom arm switching element driving signal criteria output terminal can be made equal by having established a means to transmit the output from a current detector to the high proof pressure IC according to the inverter equipment concerning the next invention It can prevent impressing a negative electrical potential difference with the circuit pattern of a current detector etc. between an upper arm switching element driving signal criteria output terminal and a bottom arm switching element driving signal criteria output terminal, and proof-pressure destruction of the high proof pressure IC can be prevented.
[0174] Since the design change of the high proof pressure IC is unnecessary, while according to the inverter equipment concerning the next invention being able to prevent destruction of the high proof pressure IC besides the above-mentioned effectiveness as the cost which hardly changes to the former is also, this invention can be applied also to the inverter equipment which used the existing high proof pressure IC, and the effectiveness that destruction of the high proof pressure IC of existing equipment can be prevented is acquired.
[0175] In not forming a current detector in single phase inverter equipment according to the inverter equipment concerning the next invention It is lost by the amount of [by the inductance produced with the conventional circuit pattern] electrical-potential-difference generating. Since the negative electrical